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PMC-4108

**Wide-Range 8-Channel
16-Bit PMC Analog Input Card**

REFERENCE MANUAL

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**SECTION 1.0
OVERVIEW**

1.1 Product Summary

The PMC-4108 is a single-width PCI mezzanine card (PMC) that provides access to eight high-level analog input channels through a standard 32-Bit, 33MHz PCI bus interface. This product conforms to the mechanical and electrical requirements of the IEEE-1386 standard for common mezzanine cards, and complies with IEEE PCI local bus specification Revision 2.2.

Eight differential analog inputs can be scanned and digitized to 16-Bit resolution at aggregate conversion rates up to 500 KSPS (thousand samples per second). The card accommodates fullscale input ranges from ± 2.5 Volts to ± 200 Volts, and withstands input overvoltages to ± 300 Volts. All inputs accept a very high common mode range of ± 200 Volts.

Digitized input data accumulates in a 64-Ksample buffer until extracted by the host through the PCI bus. A scan table controls both the scanning sequence and the input range on a channel-by-channel basis.

Input connections from the system are accepted at the front panel through a standard 50-pin 0.05" subminiature-D male connector. Power requirements consist of a single +5 Volt source obtained from the PCI bus. Figure 1.1-1 shows the general locations of major functions and components.

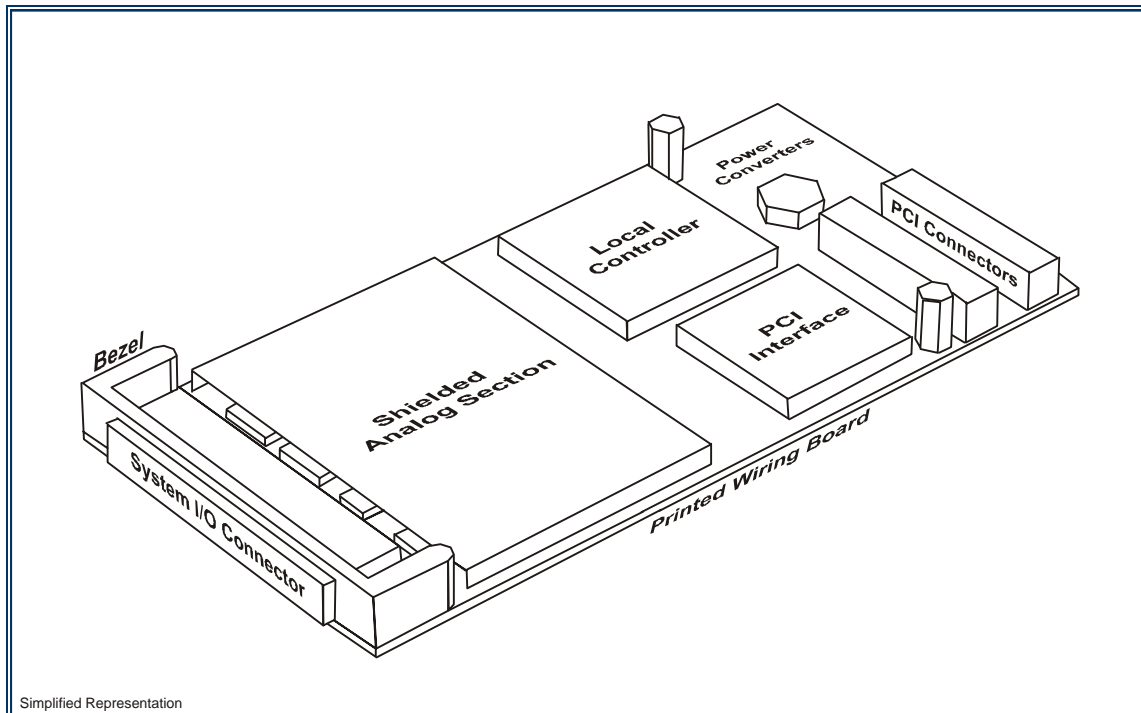


Figure 1.1-1. Physical Organization

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1.2 Mechanical Outline

This product conforms to the mechanical constraints shown in Figure 1.2-1, in compliance with the IEEE-1386 standard for common mezzanine cards.

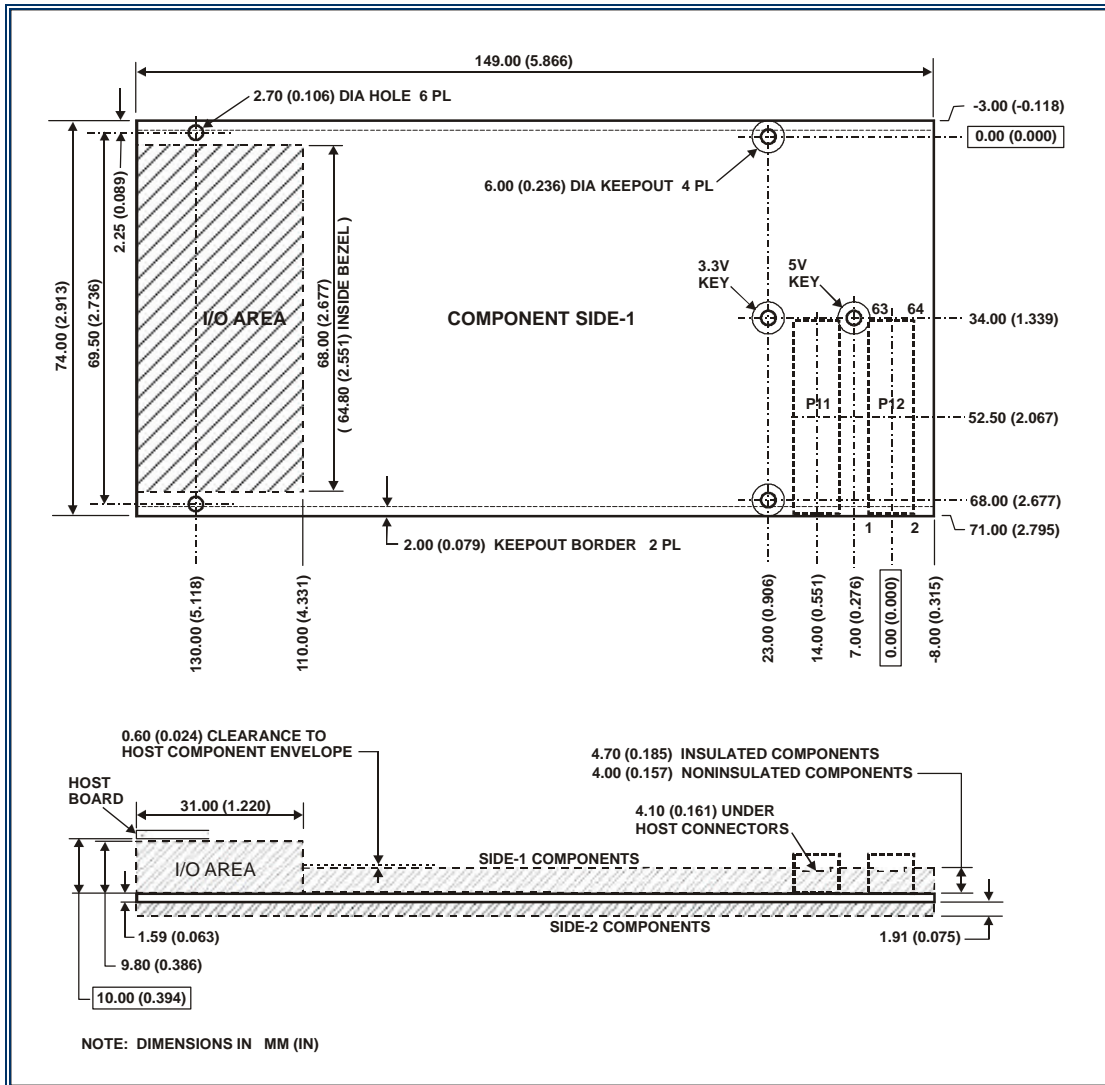


Figure 1.2-1. PMC Mechanical Detail

1.3 Document Scope

This reference manual describes the control characteristics and hardware installation requirements for the PMC-4108 card, and provides a functional description of internal hardware operation. Although occasional references are made to performance characteristics, the product specification SPEC-PMC4108 is the controlling document for performance parameters. An electrical schematic, if provided with this manual, represents the hardware configuration at the time of issue.

SECTION 2.0

CONTROL

2.1 Overview

The control interface for the PMC-4108 complies with the IEEE PCI local bus specification Revision 2.2 for a 32-bit data bus and a 33 MHz PCI clock. A PCI-9054 PLX™ PCI adapter provides communication between the PCI bus and the internal control bus. The module occupies 128 contiguous bytes of control space, and can be located on any 32 longword boundary in memory.

Local control registers, shown in Table 2.1-1, are accessed with single read or write operations, while two FIFO access registers support both single transactions and mastered DMA transactions. A single interrupt on the PCI INT-A line can respond to any of multiple selectable events.

NOTE: To ensure compatibility with subsequent firmware extensions, only zero-states should be written to control fields that are identified as "reserved."

2.2 Reset and Initialization

When a reset occurs on the PCI bus, both the PCI adapter and the local controller are initialized. The local controller autoloads configuration information from internal EPROM, and then initializes its internal registers to default values. The total time required for these operations is approximately 200-300 milliseconds.

The local controller can be initialized without affecting the configuration of either the PCI adapter or the controller, by setting the INITIALIZE control bit HIGH in the board control register (BCR), shown in Table 2.2-1. Local controller initialization requires approximately 30 milliseconds for execution, after which the control bit is cleared automatically and the local interrupt is asserted.

Upon completion of reset or initialization, the module is in the following state:

- ◆ All control registers are in their default states
- ◆ The initialization interrupt is selected and the local interrupt line is asserted
- ◆ Input clocking and triggering are disabled
- ◆ The input data buffer and scan table FIFO's are cleared (empty)
- ◆ Selected A/D converter clocking rate is 100 KSPS
- ◆ Selected scan rate is 10K scans per second
- ◆ Digital bidirectional I/O lines are configured as Direct-I/O inputs
- ◆ Digital I/O buffer is cleared and looping is disabled
- ◆ Digital I/O rate generator frequency is 16MHz.

In addition to these initial conditions, the PCI interrupt is disabled after a PCI reset occurs.

2.3 Analog Inputs

Control of the analog inputs requires the following parameters to be addressed:

- ◆ Scanning Mode; continuous or single-scan
- ◆ Input voltage range
- ◆ Scan Table, defining channel numbers and subranges
- ◆ Sample clocking source
- ◆ Scan rate source.

2.3.1 Scanning Mode

Two scanning modes are available. The CONTINUOUS SCAN MODE control bit in the BCR selects the continuous mode when HIGH, or the single-scan (burst) mode when LOW. In the continuous scanning mode, the sequence of channels defined in the scan table is scanned continuously, and all burst trigger sources are ignored.

In the single-scan, or burst, mode, a burst trigger initiates a single scan of the channels defined in the scan table. Sampling during each scan occurs at the selected sample clocking rate.

NOTE: The terms "single scan" and "burst" are used interchangeably here.

2.3.2 Input Range

The input range is determined by two range adjustment parameters, as shown in Table 2.3.2-1. Each channel can be independently assigned one of three subranges, referred to as the LOW, MID and HIGH subranges. In addition to the subrange for each individual channel, a HIGH or LOW range can be assigned independently to all even-numbered channels and to all odd-numbered channels. The total span of ranges that can be selected is from ± 2.5 Volts to ± 200 Volts.

HIGH and LOW odd/even-channel ranges are selected by the two ODD/EVEN CHANNEL LO RANGE control bits in the BCR. All even-numbered channels (0, 2, 4...) are configured in the LOW range if the EVEN CHANNEL LO RANGE control bit is HIGH, or in the HIGH range if the bit is LOW. The HIGH/LOW range of odd-numbered channels (1, 3, 5...) is controlled in the same manner by the ODD CHANNEL LO RANGE control bit.

The subrange for each channel is assigned in the scan table.

2.3.3 Scan Table

All analog input measurements are controlled by a scan table that provides considerable flexibility in defining a scanning sequence. The scan table (Table 2.3.3-1) is constructed by the user in a 256-Word FIFO buffer that is accessed through a write-only SCAN TABLE register in the local space. Each scan table location contains two fields for assigning the channel number and subrange, and a LAST CHANNEL control bit that identifies a specific sample in the scan table as the last sample in a scan. The LAST CHANNEL control bit is used only in the burst scanning mode, and is ignored in the continuous mode.

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A CLEAR SCAN TABLE control bit in the BCR clears the scan table when asserted HIGH, and then the control bit clears automatically. Write-transactions to the scan table can be single-write or mastered DMA transactions.

NOTE: Scan clocking must be disabled before the scan table can be loaded. Values written to the scan table register are ignored if input clocking is enabled. Clocking is disabled by clearing the SCAN CLOCK CONTROL field in the BCR.

After first clearing the table FIFO by asserting the CLEAR SCAN TABLE in the BCR HIGH, the table is loaded with the required scanning sequence. During scanning, the sequence of values contained in the scan table recirculates through the table FIFO.

At the beginning of each scan, the channel identified by the first value loaded into the table is the first to be digitized and loaded into the input buffer. Then the channel identified by the second value is digitized, and this sequence continues until a last-channel flag is encountered in the scan table.

If the single-scan mode is selected, the channel identified by the last-channel value is digitized, and then sampling ceases until a subsequent trigger occurs. In the continuous scanning mode, the last-value flag is ignored, and scanning continues indefinitely at the selected sample rate until disabled either by changing modes, by disabling clocking, or by initialization.

2.3.3.1 Scan Table Examples

Three channels are scanned in the example illustrated in Table 2.3.3.1-1. Channel 03 is sampled twice with the MID subrange selected. Then Channel 06 is sampled once with the LOW subrange selected, followed finally by three samples of Channel 05 on the LOW, MID, then HIGH subranges. Table 2.3.3.1-2 is a scan list for all eight inputs with various subranges, and Table 2.3.3.1-3 illustrates a complete single-burst acquisition sequence.

2.3.3.2 Single-Channel Sampling

Any single channel can be sampled continuously by loading the scan table with a single value that identifies the required channel number and subrange, and by selecting the continuous scanning mode. The continuous scanning mode is selected by setting the CONTINUOUS SCAN MODE bit HIGH in the BCR. When clocking is enabled, the selected channel is sampled continuously at the selected sampling clock rate.

Another application for single-channel sampling establishes a specific number of samples to be acquired in a burst after a trigger occurs. This is achieved by loading the scan table with consecutive duplicates of the initial value, with the total number of values equaling the required number of samples in a burst. The LAST CHANNEL FLAG is asserted HIGH in the final table value, and the single-scan scanning mode is selected by clearing the CONTINUOUS SCAN MODE bit LOW in the BCR. After clocking and scanning are enabled, each trigger initiates a single burst of readings from the same channel.

NOTE: Single-channel scanning provides the highest available sampling rate, while multichannel scanning has a somewhat lower maximum rate due to limitations in the switching speed of the multiplexer.

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2.3.4 Sample Clocking Source

When clocking is enabled, the A/D converter performs a single conversion for each occurrence of the sample clock. The conversion is completed in approximately 2.0 microseconds, after which the digitized value is loaded into the input data buffer. In the single-scan scanning mode, the first conversion in each scan commences within 60 ns of the trigger.

Table 2.3.4-1 lists the available clocking modes that are controlled with the SAMPLE CLOCK CONTROL field in the BCR. A value of zero for this field disables input sample clocking and enables PCI bus access to the scan table. In the CLOCK RATE GEN mode, a conversion commences in response to each internal sample clock.

If the EXT CLOCK INPUT mode is selected, a conversion commences at each HIGH-to-LOW transition of the external clock input from the system I/O connector. If the DIGITAL IO D00 is selected, a conversion commences at each HIGH-to-LOW transition of the external digital I/O line DIG00 in the system I/O connector.

The FORCE SAMPLE CLOCK code initiates a single A/D conversion and then clears the SAMPLE CLOCK CONTROL field.

NOTES: A 60 ns low-pulse appears at the external clock output line each time a conversion commences, regardless of which clocking and scanning modes are selected.

Sample clocking, when enabled, commences simultaneously with scan initiation.

The frequency of the internal sample clock generator is controlled by the value **Nsamp** written to the Sample Rate control register listed in Table 2.1-1. The sampling frequency **Fsamp** is determined by **Nsamp** as:

$$F_{\text{samp}} = 32,000 \div N_{\text{samp}},$$

where **Fsamp** is in kilohertz and **Nsamp** is an integer between 64 and 1,048,575. For example, an **Nsamp** value of 1000 (0x0000 03E8) produces a sample clocking frequency of 32.00 kHz. **Nsamp** values less than 64 can produce erratic performance, and are not recommended.

2.3.5 Scan Clocking Source

When the single-scan scanning mode selected and clocking is enabled, each output clock from the scan rate clock generator initiates a single scan of all inputs defined in the scan table. During each scan, conversions occur at the selected sample clock rate. Each scan proceeds until a scan table value is obtained in which the LAST CHANNEL flag is asserted HIGH. This flag causes the scan to terminate after digitizing the last channel.

Table 2.3.5-1 lists the available scan rate control modes. A value of zero for this field disables all single-scan triggers. In the SCAN RATE GEN mode, a new scan commences at each occurrence of the internal scan clock generator. If the EXT TRIG INPUT mode is selected, a new scan commences at each HIGH-to-LOW transition of the external trigger input from the system I/O connector. If the DIGITAL IO D01 is selected, a new scan commences at each HIGH-to-LOW transition of the external digital I/O line DIG01 in the system I/O connector.

Note: Asserting the CLEAR SCAN TABLE control bit in the BCR aborts any currently executing scan.

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The FORCE SCAN CLOCK code initiates a single input scan, and then clears the SCAN CLOCK CONTROL field.

NOTE: A 60 ns low-pulse appears at the external trigger output line each time a scan commences, regardless of which clocking and scanning modes are selected.

The frequency of the internal scan clock generator is controlled by the value **Nscan** written to the Scan Rate control register listed in Table 2.1-1. The scanning frequency **Fscan** is determined by **Nscan** as:

$$\mathbf{Fscan} = 32,000 \div \mathbf{Nscan},$$

where **Fscan** is in kilohertz and **Nscan** is an integer between 64 and 1,048,575. For example, a value of 10,000 (0x0000 2710) would produce a scanning clock frequency of 3.20 kHz.

The scan rate must be low enough to ensure that all samples defined in the scan table are completed between scan clocks. That is:

$$\mathbf{Fscan} < (\mathbf{Fsamp} \div \mathbf{Ntable}),$$

where **Ntable** equals the number of input samples defined in the scan table.

2.3.6 Multicard Synchronization

Multiple modules can be synchronized together to sample their inputs simultaneously, to initiate scans simultaneously, or to do both simultaneously. External wiring is required to take advantage of this feature, as described in Section 3.

For multiple-module synchronized sampling, the external clock output from one card, designated as the initiator, is connected to the external clock input of a second module, designated as a target. Multiple targets can be interconnected in the same manner to produce an indefinitely long chain of sample-synchronized modules.

To synchronize sampling among correctly interconnected modules, the control software selects the CLOCK RATE GEN sample clock mode for the initiator module, and the EXT CLOCK INPUT mode for all targets. Thereafter, each sample clock on the initiator module initiates an A/D conversion on all modules. The latency through each module is 70 ns or less.

To trigger scans simultaneously on all modules, the interconnection method described above is applied to trigger input and output connections, and the SCAN RATE GEN and EXT TRIG INPUT scan clock sources are selected for the initiator and targets, respectively.

2.3.7 Selftest Modes

Three selftest modes (Table 2.3.7-1) support verification of analog input accuracy by providing access to internal test points through the A/D converter. The Test VCAL mode connects the internal precision +2.4805 VDC reference directly to the A/D converter, and should produce a nominal value of 0xFF00 (offset binary) when read on the ±2.5 Volt input range.

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In the Test VRANGE mode, the monitored test point should return a value of 0xFF00, regardless of the selected range. The Test Zero Reference test point is analog ground, and should produce a midscale reading of 0x8000. The actual value returned in any mode is subject to the accuracy specified for the module's analog inputs.

2.4 Input Data Buffer

Analog data from the A/D converter is stored in a FIFO buffer that is accessed through the read-only Input Data Buffer register listed in Table 2.1-1. The input data buffer can be read, cleared, and monitored for the number of samples it contains. Read-transactions from the buffer can be single-read or mastered DMA transactions.

2.4.1 Organization

The input data buffer is a 64 Ksample FIFO with 17 active data bits. Each sample value (Table 2.4.1-1) consists of a 16-bit data field and a single flag bit that identifies the last channel in a scan. An empty buffer returns an indeterminate value.

2.4.2 Data Coding Format

Input data coding format can be selected as either offset binary or two's complement (Figure 2.4.2-1). The default offset binary format is selected when the BUFFER OFFSET BINARY control bit in the BCR is HIGH. Clearing the control bit LOW selects two's complement format.

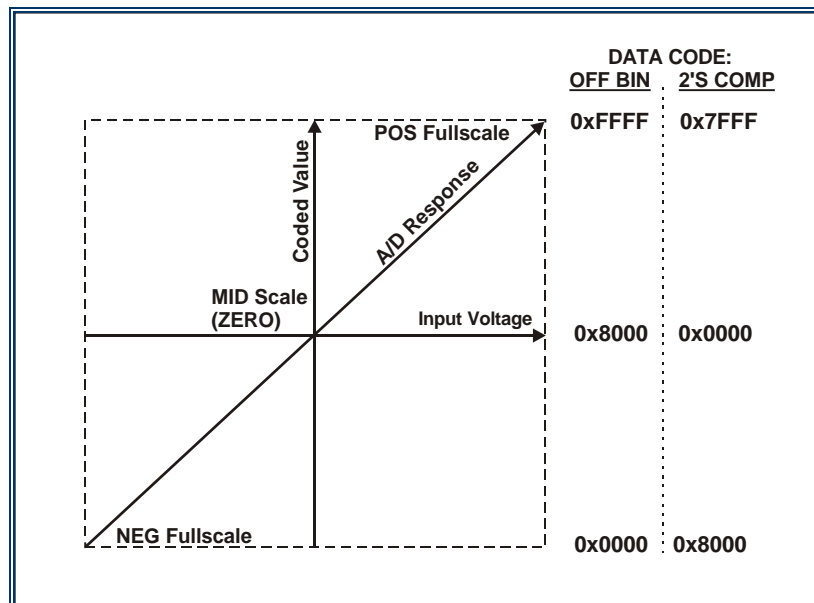


Figure 2.4.2-1. Analog Data Coding Formats

2.4.3 Buffer Control

The buffer is cleared (emptied) by asserting the CLEAR BUFFER control bit HIGH in the Buffer Operations control register (Table 2.4.3-1). The control bit clears automatically.

The THRESHOLD FLAG is asserted HIGH when the number of sample values in the buffer exceeds the value written to the BUFFER THRESHOLD field. A threshold value of 0x0000 produces a LOW threshold flag when the buffer is empty, and a value of 0xFFFE asserts the flag HIGH when the buffer is FULL. An interrupt can be generated on both LOW-to-HIGH and HIGH-to-LOW transitions of the threshold flag.

2.4.4 Buffer-Used Register

As data flows to and from the input data buffer, the number of values contained within the buffer is reported through the read-only BUFFER USED register listed in Table 2.1-1.

2.5 Digital Input/Output

2.5.1 Digital I/O Control Register

System digital I/O signals are controlled through the Digital I/O control register shown in Table 2.5.1-1. A single external output line follows the DIG AUX 01 OUTPUT control bit, and the DIG AUX 00 INPUT status bit follows a single external input line. Status bits D08-D11 are read-only flags that indicate the extent to which the digital I/O buffer is filled.

2.5.2 Bidirectional Digital Buffer

Eight bidirectional lines provide a byte-wide data FIFO port that is accessed through the Digital I/O Buffer register listed in Table 2.1-1. Bits D00-D07 of the buffer correspond to external digital I/O lines DIG00-07 respectively, with no logic inversions. The buffer supports both single-read/write and mastered DMA transactions. Clocking of the buffer is enabled by setting the ENABLE CLOCKING control bit HIGH in the digital I/O control register. If the DIRECT I/O control bit in the digital I/O control register is HIGH, bidirectional digital I/O data bypasses the digital I/O FIFO, and the clocking input is ignored.

The digital I/O buffer is organized as an 8-bit by 256-byte FIFO, the direction of which is determined by the state of the DATA DIRECTION OUT control bit in the digital I/O control register. If the DATA DIRECTION OUT control bit is LOW, external lines DIG00-07 are configured as inputs. In this case, the input of the FIFO accepts input data from the external lines DIG00-07, and the FIFO output is available to the PCI bus. The BUFFER LOOP control bit in the digital I/O control register has no effect while the external bidirectional lines are configured as inputs.

If the DATA DIRECTION OUT control bit is HIGH, external lines DIG00-07 become digital outputs, and the FIFO output is available to external lines DIG00-07. If the DIRECT I/O control bit in the digital I/O control register is LOW, the input of the FIFO accepts data from the PCI bus. If the BUFFER LOOP control bit in the digital I/O control register is HIGH while the port is configured as an output port, data already present in the FIFO recirculates within the FIFO, and write transactions from the PCibus are ignored.

NOTE: The output of the digital I/O FIFO retains either (a) the first value written to the FIFO after the FIFO is cleared, or (b) the last value read from the FIFO. Clearing the FIFO does not remove the output value, and least one clock is required to fetch a new value.

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Table 2.5.2-1 summarizes the behavior of the byte-wide digital I/O port in its various operating modes. Table 2.5.2-2 lists two simple examples of typical operating sequences.

2.5.3 Digital I/O Clocking

When the bidirectional digital I/O lines are configured as an output port, data from the digital I/O buffer is clocked to the system I/O connector by a digital rate generator. This generator is controlled by the 16-bit Digital Rate Gen control register listed in Table 2.1-1. For a value **Ndig** in the register, the digital I/O buffer clocking rate **Fdig** is:

$$\mathbf{Fdig} = 32 \cdot \mathbf{Ndig},$$

where **Fdig** is in megahertz, and **Ndig** can be any integer between 2 and 65535.

If the bidirectional I/O lines are configured as an input port, data from the I/O lines is clocked into the digital I/O buffer at the rate determined by the digital rate generator.

2.6 Interrupts

Specific events occurring within the module can be selected to produce an interrupt request on the single PCI interrupt line (INT-A). For the interrupt to be active however, it must first be enabled through the PCI adapter.

To enable interrupts from the PCI adapter:

- a. Determine the configuration address of the runtime interrupt status control register:
 - ◆ Read the PCI base address in PCI configuration space. The offset for the base address is 0x10 for memory-mapped configurations, or 0x14 for I/O-mapped configurations.
 - ◆ Add 0x68 to the base address to obtain the address of the interrupt status control register.
- b. Read the interrupt status control register, and write the value back to the register after logically OR'ing the pattern 0x0000 0900 to the value.

2.6.1 Organization

Interrupt control fields in the Interrupt Control register (Table 2.6-1) are organized into a selection field and a response field. Each available interrupt event has both a selection control bit and a corresponding response status bit. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit itself, or by clearing the associated selection bit.

NOTE: The interrupt response status bits can only be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The PCI interrupt output from the module is asserted if any response bit in the interrupt control register is asserted (and if the interrupt is enabled in the PCI adapter). To clear the interrupt, all response bits must be cleared.

2.6.2 Event Detection

Interrupt event detection is edge-activated on a transition of the selected event from false to true. Once asserted, each response status bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

2.7 Direct Memory Access

For those registers that support DMA, PCI data transfers are executed with the module acting as DMA master. The local configuration registers listed in Table 2.7-1 control the DMA configuration for data transfers both to and from the module.

2.8 Autocalibration

To ensure full conformance with the product specification, autocalibration should always be invoked after power has been applied to the board, or after a software or hardware reset has occurred. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs immediately after power is applied.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration, which has a duration of approximately 3-5 seconds, is indicated by the AUTOCAL bit clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event. Read/write accesses from the PCI bus during autocalibration can produce unpredictable results, and are not recommended. The software-controlled board configuration that exists when autocalibration is invoked is restored when autocalibration has been completed.

If a board is defective, the autocalibration process may be unable to successfully calibrate all analog channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS after autocalibration indicates that the calibration was successful.

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2.9 Control Section Tables

Table 2.1-1 Local Control Registers

LOCAL ADDR	ACCESS MODE	REGISTER	DEFAULT	DESCRIPTION
0x00	R/W	BOARD CONTROL	0x0002 D008	Board Control Register (BCR)
0x04	R/W	INTERRUPT CONTROL	0x0000 0101	Interrupt event selection and status
0x08	RO (DMA)	INPUT DATA BUFFER	---	Input Data FIFO Buffer
0x0C	R/W	BUFFER OPERATIONS	0x0000 FFFE	Input buffer control and status threshold
0x10	RO	BUFFER USED	0x0000 0000	Number of samples in the input data buffer
0x14	---	(Reserved)	0x0000 0000	(Inactive)
0x18	WO(DMA)	SCAN TABLE	0x0000 0000	Analog input scan table. Channel, subrange
0x1C	R/W	SAMPLE RATE	0x0000 0140	Sample rate control divisor
0x20	R/W	SCAN RATE	0x0000 0C80	Scan rate control divisor
0x24	R/W	DIGITAL I/O CONTROL	0x0000 0110	Digital I/O port control
0x28	R/W(DMA)	DIGITAL I/O BUFFER	0x0000 00XX	Digital I/O FIFO buffer
0x2C	R/W	DIGITAL RATE GEN	0x0000 0002	Digital I/O buffer rate generator divisor
0x30	---	F/W Revision *	---	*
0x34	---	Autocal Values *	---	*
0x38-0x7F	---	(Reserved)	---	(Inactive)

R/W = Read/Write; RO = Read-Only; WO = Write-Only; X = Undefined state.

* Test registers; shown for reference only.

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Table 2.2-1. Board Control Register; Offset 0x00

DATA BIT	DESIGNATION	DEFAULT	DESCRIPTION
D00-01	SELFTEST MODE	0x0	Configures the analog input channels for normal operation or selftest modes.
D02	(Reserved)	0	---
D03	CONTINUOUS SCAN MODE	1	Selects continuous analog input scanning when HIGH, single-scan (burst) scanning when LOW.
D04-06	SAMPLE CLOCK CONTROL	0x0	Controls the A/D converter sample clock source and mode.
D07	(Reserved)	0	---
D08-10	SCAN CLOCK CONTROL	0x0	Controls the scan rate clock source and mode
D11	(Reserved)	0	---
D12	BUFFER OFFSET BINARY	1	Selects two's complement input data format when LOW, or offset binary format when HIGH.
D13 *	BUFFER THRESHOLD FLAG	0	Asserted HIGH when buffer contents exceed the assigned threshold. Duplicated in the Buffer Operations control register.
D14	EVEN CHANNEL LO RANGE	1	Configures all even-numbered channels in the LOW range when HIGH, or in the HIGH range when LOW
D15	ODD CHANNEL LO RANGE	1	Configures all odd-numbered channels in the LOW range when HIGH, or in the HIGH range when LOW
D16	AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.
D17 *	AUTOCAL PASS	1	Indicates a successful autocalibration when HIGH, or an autocalibration failure when LOW.
D18	CLEAR SCAN TABLE	0	Clears the scan table FIFO. Aborts current scan. **
D19	INITIALIZE	0	Initializes the board when asserted. Sets all defaults.
D20-31	(Reserved)	0x0	Read-Only, returns all-zero value.

* Read-Only. All other bits are Read/Write. ** Control bit clears automatically.

Table 2.3.2-1. Analog Input Range

HIGH/LOW RANGE	SUBRANGE	EFFECTIVE ANALOG INPUT RANGE
LOW	LOW	±2.5 Volts
	MID	±5 Volts
	HIGH	±10 Volts
HIGH	LOW	±50 Volts
	MID	±100 Volts
	HIGH	±200 Volts

* Default value for field.

PRELIMINARY

Table 2.3.3-1. Scan Table Register; Offset 0x18

CONTROL BITS	DESIGNATION	FUNCTION *
D00-02	CHANNEL SELECT	Selects Channel 0-8.
D03	(Reserved)	---
D04-05	SUBRANGE	Selects subrange as: 0 -> LOW subrange 1 -> MID subrange 2 -> HIGH subrange 3 -> HIGH subrange
D06-07	(Reserved)	---
D08	LAST CHANNEL	Set HIGH for the last channel in a scan.
D11-31	(Reserved)	---

* All fields are write-only, and return a zero value when read from the bus.

2.3.3.1-1. Scan Table Example A

FIFO SEQUENCE	LAST CHANNEL	SUBRANGE	INPUT CHANNEL	SCAN TABLE VALUE
0 (first)	NO	MID	3	0x013
1	NO	MID	3	0x013
2	NO	LOW	6	0x006
3	NO	LOW	5	0x005
4	NO	MID	5	0x015
5 (last)	YES	HIGH	5	0x125

2.3.3.1-2. Scan Table Example B

FIFO SEQUENCE	LAST CHANNEL	SUBRANGE	INPUT CHANNEL	SCAN TABLE VALUE
0 (first)	NO	HIGH	3	0x023
1	NO	LOW	4	0x004
2	NO	MID	2	0x012
3	NO	HIGH	5	0x025
4	NO	MID	1	0x011
5	NO	HIGH	6	0x026
6	NO	LOW	0	0x000
7 (last)	YES	HIGH	7	0x127

PRELIMINARY

Table 2.3.3.1-3. Scan Table Example C; Single-Burst

This sequence acquires 16 HIGH-subrange samples for each input channel, thereby providing a total of 128 (16*8) samples. Once established, the acquisition sequence can be repeated by writing a single value to the BCR. Repetition of the sequence can continue until the input buffer is full.

To modify the sequence for another subrange, change the D04-07 nibble in each scan-table value from "2" to "1" for the MID subrange, or to "0" for the LOW subrange.

STEP	REGISTER	OFFSET	VALUE	OPERATION
1	BCR	0x00	0x0006 D010	Select the system input lines as inputs to the ADC. Select the clock generator as the sample clocking source. Clear the SCAN CLOCK CONTROL field in the BCR. Clear the scan table.
2	SAMPLE RATE	0x1C	0x0000 0140	Adjust the sample rate to 100 KSPS
3	SCAN TABLE (Eight groups, with 16 samples of a single channel in each group)	0x18	0x0000 0020 *	CH 00, HIGH subrange, 1st 16-value group in scan table
			0x0000 0021 *	CH 01, HIGH subrange, 2nd group
			0x0000 0022 *	CH 02, HIGH subrange, 3rd group
			0x0000 0023 *	CH 03, HIGH subrange, 4th group
			0x0000 0024 *	CH 04, HIGH subrange, 5th group
			0x0000 0025 *	CH 05, HIGH subrange, 6th group
			0x0000 0026 *	CH 06, HIGH subrange, 7th group
			0x0000 0027 **	CH 07, HIGH subrange; 8th group 0x0000 0127 for final (LAST) value.
4	BCR	0x00	0x0002 D310	Force a single scan-table scanning sequence, by writing a "3" to the SCAN CLOCK CONTROL field in the BCR. Acquire 16 samples for each of all eight channels
***	BCR	0x00	0x0002 D310	Repeat. Acquire 16 samples for each of all eight channels
***	BCR	0x00	0x0002 D310	Repeat. Acquire 16 samples for each of all eight channels

* First of 16 consecutive identical values.

** 15 identical values, terminated by a value that includes the LAST-CHANNEL flag.

*** Single operation required to repeat the acquisition cycle.

PRELIMINARY

Table 2.3.4-1. BCR Sample Clock Control Field

FIELD VALUE	DESIGNATION	ADC SAMPLE-INITIATION EVENT
0x00 *	SAMPLING DISABLED	Input sampling is disabled. The PCI bus has access to the scan table FIFO.
0x01	CLOCK RATE GEN	** Sample clock rate generator.
0x02	EXT CLOCK INPUT	** HIGH-to-LOW transition of the external clock input.
0x03	FORCE SAMPLE CLOCK	** A/D converter is clocked when this value is written to this field. The value of this field returns to 0x0 when the conversion is completed.
0x04	DIGITAL I/O D00	** HIGH-to-LOW transition of digital I/O line DIG00.
0x04-07	(Reserved)	---

* Default value for field. ** PCI access to the scan table FIFO is disabled.

Table 2.3.5-1 BCR Scan Clock Control Field

FIELD VALUE	DESIGNATION	SCAN INITIATION EVENT
0x00 *	DISABLED	---
0x01	SCAN RATE GEN	Each output clock from the scan clock rate generator.
0x02	EXT TRIG INPUT	HIGH-to-LOW transition of the external trigger input.
0x03	FORCE SCAN CLOCK	A single scan is initiated when this value is written to this field. The value of this field returns to 0x0 when the scan is completed.
0x04	DIGITAL I/O D01	HIGH-to-LOW transition of digital I/O line DIG01.
0x04-07	(Reserved)	---

* Default value for field.

Table 2.3.7-1. BCR Selftest Mode Control Field

SELFTTEST MODE	DESIGNATION	ADC INPUT SOURCE
0x00 *	System Analog Inputs	System analog input channels.
0x01	Test VCAL	Internal +2.48 Volt reference voltage.
0x02	Test VRANGE	Internal subrange 99.2% fullscale reference voltage.
0x03	Test Zero Reference	Internal midscale (zero-voltage).reference..

* Default value for field.

PRELIMINARY

Table 2.4.1-1. Input Data Buffer Register ; Offset 0x08

DATA BIT	DESIGNATION	FUNCTION
D00-15	INPUT DATA	Analog input data in offset binary or two's complement format
D16	LAST CHANNEL	Identifies the last channel in a scan.
D17-31	(Reserved)	Read-Only, returns all-zero value.

Table 2.4.3-1. Buffer Operations Control Register; Offset 0x0C

CONTROL BITS	DESIGNATION	DEFAULT	FUNCTION *
D00-15	BUFFER THRESHOLD	0xFFFE	Input buffer flag threshold. The buffer threshold flag is asserted HIGH when the number samples in the data buffer exceeds this value.
D16	THRESHOLD FLAG	0	Asserted HIGH when the number of sample values in the data buffer exceeds the buffer threshold.
D17	CLEAR BUFFER	0	The buffer is cleared (emptied) when this bit is asserted HIGH. This control bit returns to zero automatically.
D18-31	(Reserved)	0x000	Read-Only, returns all-zero value.

* All control bits are READ/WRITE unless indicated otherwise

Table 2.5.1-1. Digital I/O Control Register; Offset 0x24

BITS	DESIGNATION	DEFAULT	FUNCTION *
D00	DATA DIRECTION OUT	0	Configures the bidirectional data lines as outputs from D00-07 of this register when asserted HIGH, or as inputs to this register when LOW.
D01	BUFFER LOOP	0	Closes the buffer for data recirculation when HIGH, opens the buffer for pass-thru operation when LOW.
D02	CLEAR DIGITAL BUFFER	0	Clears the digital I/O buffer. (Bit clears automatically).
D03	ENABLE CLOCKING	0	Enables digital I/O buffer clocking.
D04	DIRECT I/O	1	Routes I/O data around (bypasses) the digital I/O FIFO
D05	(Reserved)	---	---
D06	DIG AUX 01 OUTPUT	0	Output-only digital line
D07	DIG AUX 00 INPUT	0	Read-Only. Input-only digital line
D08	BUFFER EMPTY	1	Read-Only. HIGH only when the digital buffer is empty.
D09	BUFFER 1/4 FULL	0	Read-Only. HIGH when the buffer is 1/4 full or more.
D10	BUFFER 3/4 FULL	0	Read-Only. HIGH when the buffer is 3/4 full or more.
D11	BUFFER FULL	0	Read-Only. HIGH only when the buffer is full.
D12-31	(Reserved)	---	Read-Only, returns all-zero value.

* All control bits are READ/WRITE unless indicated otherwise

PRELIMINARY

Table 2.5.2-1. Digital I/O FIFO Buffer; Offset 0x28

DATA DIRECTION	PCibus TRANSACTION	BUFFER LOOP	DIRECT I/O	DATA ACTIVITY
INPUT	READ	Don't Care	LOW	PCibus reads the digital I/O FIFO.
INPUT	READ	Don't Care	HIGH	DIRECT-READ MODE: (Default) PCibus reads directly from the external digital I/O lines
INPUT	WRITE	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus data is ignored.
OUTPUT	WRITE	Don't Care	HIGH	DIRECT-WRITE MODE: PCibus writes directly to the external digital I/O lines.
OUTPUT	WRITE	LOW	LOW	PASSTHRU MODE: PCibus writes to the digital I/O FIFO. External digital I/O lines follow the FIFO output.
OUTPUT	WRITE	HIGH	LOW	RECIRCULATION MODE (Looping): PCibus data is ignored. Data already present in the FIFO recirculates. External digital I/O lines follow the FIFO output.
OUTPUT	READ	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus reads the previous value written to the port.

Table 2.5.2-2. Typical Digital I/O Operation

CLOCKED OUTPUT PORT		CLOCKED INPUT PORT	
STEP	OPERATION	STEP	OPERATION
1 *	Configure as an output port. (DATA DIRECTION OUT = HIGH) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)	1 *	Configure as an input port. (DATA DIRECTION OUT = LOW) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)
2	Load the buffer with a pattern sequence.	2	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)
3	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)	3	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)
4	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)	4	The buffer begins to fill with data from the digital I/O port.
5	Data from the buffer begins to clock to the digital I/O port. If looping has not been selected, the buffer accepts subsequent data from the PCI bus.		

* Adjust all digital I/O control register bits simultaneously.

** Do not clear the buffer again at this point. For looping (periodic function generation), set BUFFER LOOP = HIGH.

PRELIMINARY

Table 2.6-1 Interrupt Control Register; Offset 0x04

CONTROL BITS	INTERRUPT EVENT	FUNCTION
D00	Initialization completed	Interrupt event selection. Enables assertion of the corresponding event flag (below) when the selected event occurs.
D01	Autocal completed	
D02	Buffer Threshold, LOW-to-HIGH transition	
D03	Buffer Threshold, HIGH-to-LOW transition	
D04	Scan Trigger event	
D05	Scan Completed	
D06	Digital buffer 1/4-Full HIGH-to-LOW transition	
D07	Digital buffer 3/4-Full LOW-to-HIGH transition	
D08	Initialization completed	Interrupt response. Asserted HIGH when a selected interrupt (above) occurs. Remains HIGH until cleared LOW. The PCI bus INT A interrupt is asserted while any event flag in this register is asserted..
D09	Autocal completed	
D10	Buffer Threshold, LOW-to-HIGH transition	
D11	Buffer Threshold, HIGH-to-LOW	
D12	Scan Trigger event	
D13	Scan Completed	
D14	Digital buffer 1/4-Full HIGH-to-LOW transition	
D15	Digital buffer 3/4-Full LOW-to-HIGH transition	
D16-31	(Reserved)	

Table 2.7-1. DMA Control Registers

CONFIGURATION REGISTER	OFFSET*	DMA FUNCTION	COMMENTS and TYPICAL VALUES
PCI Status and Command	0x04	Bus mastering selection.	Logically OR 0x0004 for bus mastering.
DMA-0 Mode	0x80	32-Bit bus, Interrupt on done, nonincrementing, local bursting, DMA Chan-0	0x0002 0D43
DMA-0 PCI Address	0x84	Initial PCI data address	Application-dependent
DMA-0 Local Address	0x88	Initial local address	Local address of data register (Table 2.1-1)
DMA -0Transfer Byte Count	0x8C	Number of bytes in transfer	Application-dependent
DMA Descriptor Counter	0x90	Transfer direction	0x0000 0000, PCI to card (write) 0x0000 000A, Card to PCI (read)
DMA-0 Command Status	0xA8	Enable/initiate transfer	0x0000 0001 to enable transfer 0x0000 0003 to initiate transfer

* From base address.

SECTION 3.0 HARDWARE INSTALLATION

3.1 System Configuration

A typical installation of a PMC I/O module involves several fundamental tasks, namely:

- ◆ Configuration of the PMC module
- ◆ System cabling and connections
- ◆ Physical installation of the PMC module on the PMC host board
- ◆ Maintenance.

The configuration of the PMC-4108 is established at the factory, and no electrical modifications are required in the field. This section provides specific information and guidelines pertaining to the remaining installation tasks. Contact Sales at Rymic Systems if prewired or custom cable assemblies are required.

3.1.1 I/O Connections

Pin assignments for the System Input/Output connector are tabulated in Table 3.1.1-1 located at the end of this section. Figure 3.1.1-1 shows the physical arrangement of the connector, which is a 68-Pin 2-Row 0.050-inch subminiature connector that is designed to mate with Robinson-Nugent Model P50E-068-S-TG or equivalent cable socket connector. Unused pins can be left disconnected in most applications, but the grounding of unused analog input lines will minimize the injection of noise into the card when operating in high-noise environments.

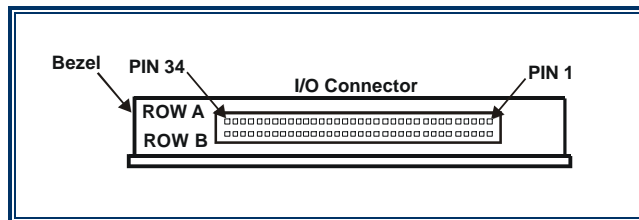


Figure 3.1.1-1. System I/O Connector

3.1.2 System Cabling

If discrete-wire system cabling is used, analog input lines should be arranged into twisted pairs, with the HI and LO inputs for each channel twisted together. If ribbon cable is used, the wire sequence is ordered in a manner that positions each HI/LO input pair as adjacent wires within the cable.

NOTE: The PMC-4108 card will accept analog input potentials up to 300 Volts relative to the INPUT RTN pins, which also are at the internal PCibus ground potential. Selection of cabling components must ensure that the insulation breakdown voltage ratings for the cable and connectors are suitable for the intended application.

Digital I/O lines also should be configured as twisted pairs, with each digital line twisted with a DIG RTN (digital return) line. In a ribbon cable, each digital signal line in the cable is positioned adjacent to a DIG RTN line.

3.2 Analog Inputs

System connections to each of the analog input channels can be configured independently for either differential or single-ended operation. Single-ended operation is recommended only for input sources that are isolated both from each other and from the system ground, or for inputs that share a common ground that is isolated from the primary system ground. The isolation need not be absolute or galvanic, but leakage resistances between isolated grounds should be high enough to ensure that ground loops do not introduce significant error potentials between input returns. An isolation resistance of several K-Ohms or higher usually is sufficient.

Differential operation of analog inputs minimizes the measurement errors introduced by ground loops or interground potentials in the system. With its very high common-mode voltage range of 200 Volts above or below system ground, the PMC-4108 will operate reliably in systems that could cause catastrophic damage to I/O modules that have the usual common mode range of 10-15 Volts.

The signal of interest from an analog source is the voltage developed between the source output, designated here as the HI line, and the source return, designated here as the LO line. Figure 3.2-1 shows this signal as **Vsig**. In most systems however, an extraneous "common mode" voltage **Vcm** exists between the source return and the primary ground in the system. Consequently, measuring the source HI line relative to system ground produces a value that includes the common mode error, instead of only the desired voltage **Vsig**.

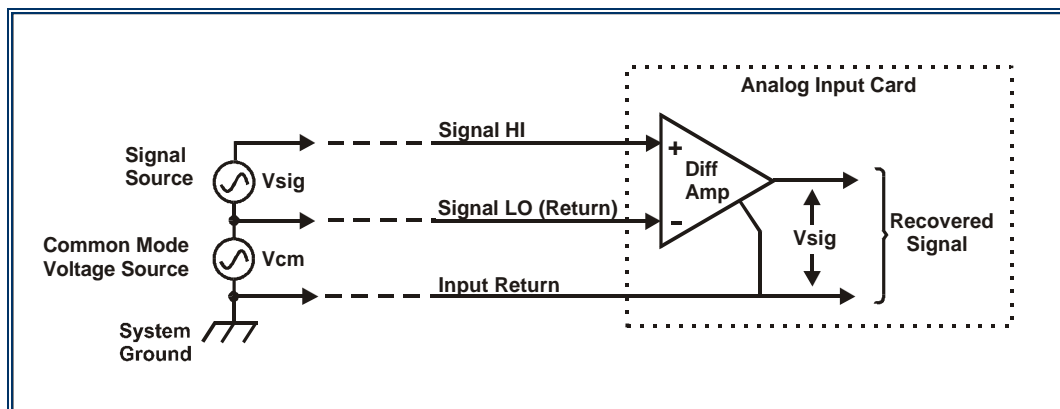


Figure 3.2-1. Analog input Channel

The differential amplifier removes the common mode error voltage and produces an output value equal to V_{sig} . The ability of the differential amplifier to reject the common mode error is indicated by the common mode rejection ratio (CMRR) contained in the product specification. The CMRR represents the ratio of the actual common mode voltage acting on a channel, to the residual common mode error present in the recovered signal.

NOTE: A formal definition specifies "common mode voltage" as the voltage between system ground and the midpoint of the source signal lines. Due to the complexity of illustrating common mode voltage in this manner, most application literature instead uses the simpler definition indicated in Figure-3.2-1.

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3.2.1 Differential Operation

For operation in differential mode, the HI input of each channel is connected to the output line from the associated signal source, and the LO input is connected to the return line. To minimize common mode noise, and to control the range of common mode voltages present in the input channels, the module's Input Return usually is connected to system ground.

If all sources share a common ground or return, the LO inputs can be connected together as shown in Figure 3.2.1-1a. However, a more reliable arrangement is shown in Figure 3.2.1-1b, in which all sources are assumed to be operating at different common mode voltages.

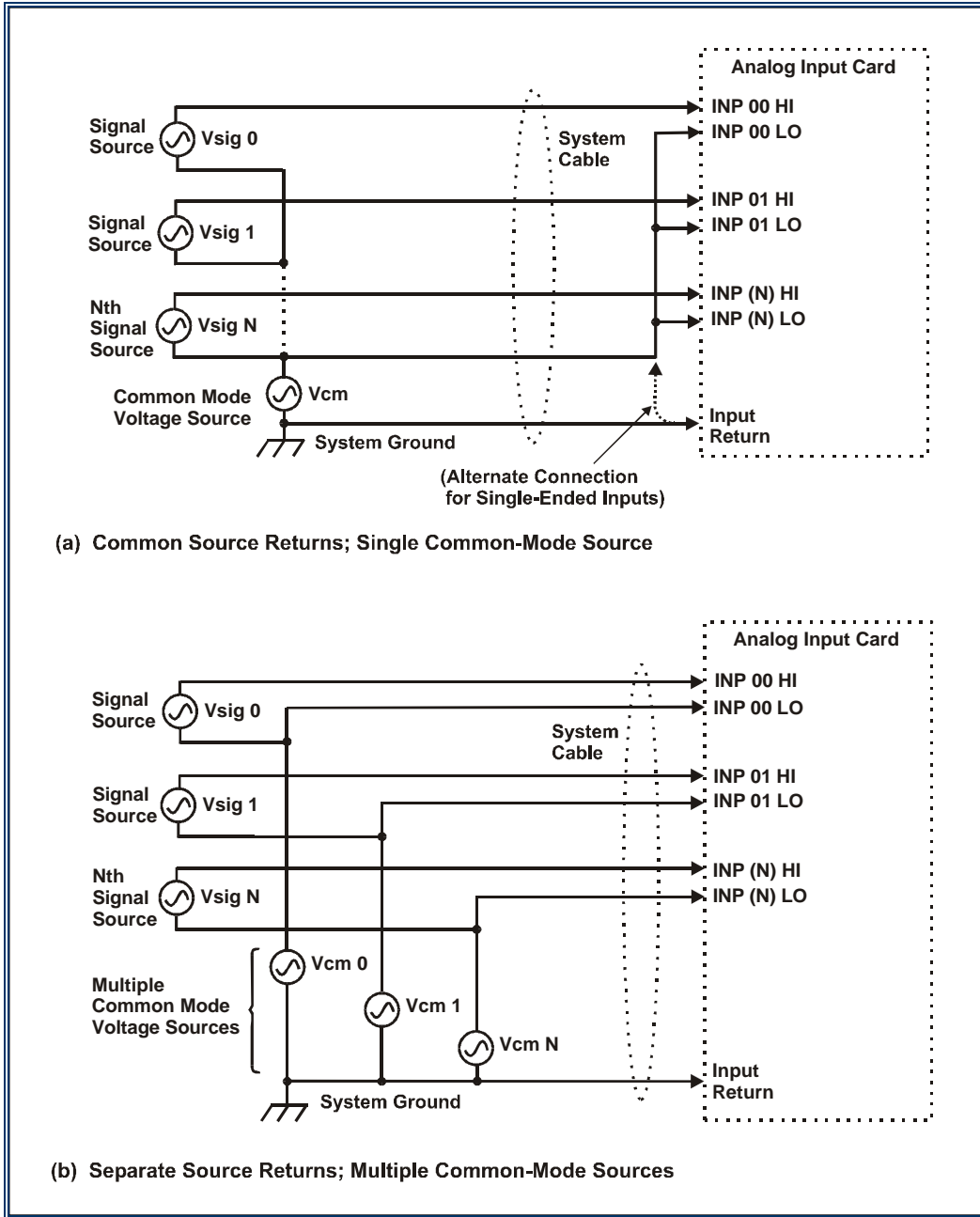


Figure 3.2.1-1. Analog Input Configurations

3.2.2 Single-Ended Operation

For single-ended channels, the HI input is connected to the signal source output line, and the LO input is connected to INPUT RTN, which in turn is connected to system ground. This configuration is indicated in Figure 3.2.1-1a, by the dashed connection at the input return connection to the input card.

NOTE: As indicated earlier, single-ended operation is suitable only for specific applications in which the input return connection is isolated from system ground. Single-ended operation with nonisolated signal sources can cause significant measurement errors and noise, as well as producing potentially damaging levels of ground current through the module's input return.

3.3 External Clock and Trigger

External clocking and burst synchronization can be implemented through the control software. If either or both of these features are to be implemented, the card must be wired accordingly.

3.3.1 Clock and Trigger Inputs

To connect the card for external clocking, connect the external clock source to the CLOCK INPUT pin, and the clock source return to DIG RTN. Similarly, for external burst synchronization, connect the synchronization source to the SYNC INPUT pin. The CLOCK and SYNC inputs accept standard TTL levels, and provide an internal 4.7K pullup resistance to +5 Volts. Both inputs are active on the falling (LOW) edges of the input signals.

3.3.2 Multicard Clocking and Scan Triggering

For multicard synchronous analog input sampling, one of the cards is software-designated as the **initiator**, and the remaining cards are designated as **targets**. If external clock and trigger sources are to be used, the clock and trigger inputs for the initiator are connected as described in Paragraph 3.3.1. If external signals are not required, the clock and trigger input connections at the initiator should be left disconnected.

The CLOCK OUTPUT signal from the initiator is connected to the CLOCK INPUT pin of one of the target cards, designated as Target-1. If more than one target card is present, the CLOCK OUTPUT from Target-1 is connected to the CLOCK INPUT pin of TARGET-2, and this sequence is repeated for all remaining target cards. The CLOCK OUTPUT from the last target in the chain is not connected.

For multicard synchronous scan triggering, the TRIG OUTPUT and TRIG INPUT connections between cards are configured as described above for synchronous input sampling..

3.4 Digital Input and Output

Digital lines DIG 00 through DIG 07 are bidirectional, with the signal direction controlled by the control software. DIG AUX 00 is a digital input-only pin, and DIG AUX 01 is a digital output-only pin. DIG AUX 00 and DIG 00 through DIG 07 are provided with internal 4.7K pullup resistors to +5 Volts. All ten digital lines respond to standard TTL levels.

3.5 Physical Installation

Before removing the PMC module from the protective antistatic shipping envelope, ensure that the host board on which the module is to be installed is ready to receive the module. The host panel opening and the mating mezzanine connectors should be free of obstructions such as protective covers and filler panels. After removing the PMC module from the antistatic shipping envelope, remove and save the mounting screws that may be installed in the bezel and standoffs.

Position the PMC module above the host as shown in Figure 3.5-1, with the PCI mezzanine connectors facing the host board, and with the I/O connector and bezel oriented toward the front panel of the host. Carefully insert the bezel of the module through the appropriate opening in the host panel, and align the PCI mezzanine connectors at the rear of the module with the mating connectors on the host. Press the rear of the module carefully but firmly downward onto the host until the bezel and the standoffs are seated against the host board. Verify that the PCI connectors have mated correctly.

Install the four 2.5mm mounting screws supplied with the module, through the host board and into the bezel and the two standoffs on the module. This completes the physical installation of the PMC module.

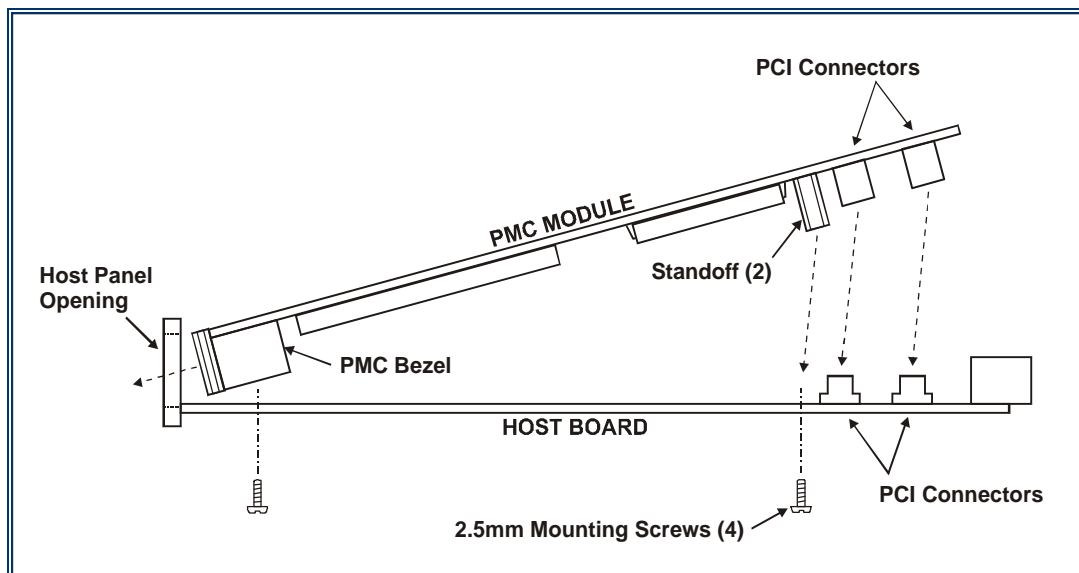


Figure 3.5-1. Physical Installation

3.6 Maintenance

Aside from the usual care associated with precision electronic equipment, this product requires no scheduled maintenance operations. In environments that contain high levels of dust, smoke or other airborne particulate materials, the module should be cleaned periodically to prevent the accumulation of surface deposits that can reduce the ability of power components to dissipate excess heat.

3.7 Internal Reference Test Point

The internal calibration reference that is used to calibrate all analog input channels during autocalibration is available between the ANA AUX HI (+) and ANA AUX LO (-) pins of the I/O connector. Under normal conditions, this reference should not require adjustment. However, if module accuracy appears to degrade, verify that the voltage between these pins is $+2.4805 \pm 0.0005$ VDC.

PRELIMINARY

Table 3.1.1-1. System I/O Connector Pin Functions

PIN	FUNCTION	PIN	FUNCTION
1A	DIG RTN	1B	DIG RTN
2A	TRIG INPUT	2B	TRIG OUTPUT
3A	DIG RTN	3B	DIG RTN
4A	CLOCK INPUT	4B	CLOCK OUTPUT
5A	ANA AUX HI	5B	DIG RTN
6A	ANA AUX LO	6B	DIG 00
7A	INPUT RTN	7B	DIG RTN
8A	INPUT RTN	8B	DIG 01
9A	ANA INP 00 LO	9B	DIG RTN
10A	ANA INP 00 HI	10B	DIG 02
11A	ANA INP 01 LO	11B	DIG RTN
12A	ANA INP 01 HI	12B	DIG 03
13A	ANA INP 02 LO	13B	DIG RTN
14A	ANA INP 02 HI	14B	DIG 04
15A	ANA INP 03 LO	15B	DIG RTN
16A	ANA INP 03 HI	16B	DIG 05
17A	ANA INP 04 LO	17B	DIG RTN
18A	ANA INP 04 HI	18B	DIG 06
19A	ANA INP 05 LO	19B	DIG RTN
20A	ANA INP 05 HI	20B	DIG 07
21A	ANA INP 06 LO	21B	DIG RTN
22A	ANA INP 06 HI	22B	DIG AUX 00 (Input)
23A	ANA INP 07 LO	23B	DIG RTN
24A	ANA INP 07 HI	24B	DIG AUX 01 (Output)
25A	INPUT RTN	25B	DIG RTN
26-34A	INPUT RTN	26-34B	DIG RTN

SECTION 4.0 FUNCTIONAL DESCRIPTION

This functional description provides a brief overview of the interfaces, internal functions and operating principles that constitute the PMC-4108 module.

4.1 External Interfaces

Two electrical interfaces provide connections between the PMC-4108 module and external system components. The host board controls the module through two PCI bus connectors that mate with two corresponding connectors located on the host (Figure 4.1-1). These connectors provide a standard 32-bit, 33 MHz PCI control interface that conforms to the IEEE PCI local bus specification Revision 2.2. The PCI interface also supplies +5 VDC power for the module, and passes measurement data and various board status information back to the host.

A system input/output connector supplies the second electrical interface, which provides connections to system signals that are external to both the host and the host cardcage. The I/O connector is located in an access opening in the front panel of the host board, and is designed to interface electrically and mechanically with conventional system cabling. All analog inputs, digital signals and external clock and trigger signals pass through the system I/O connector.

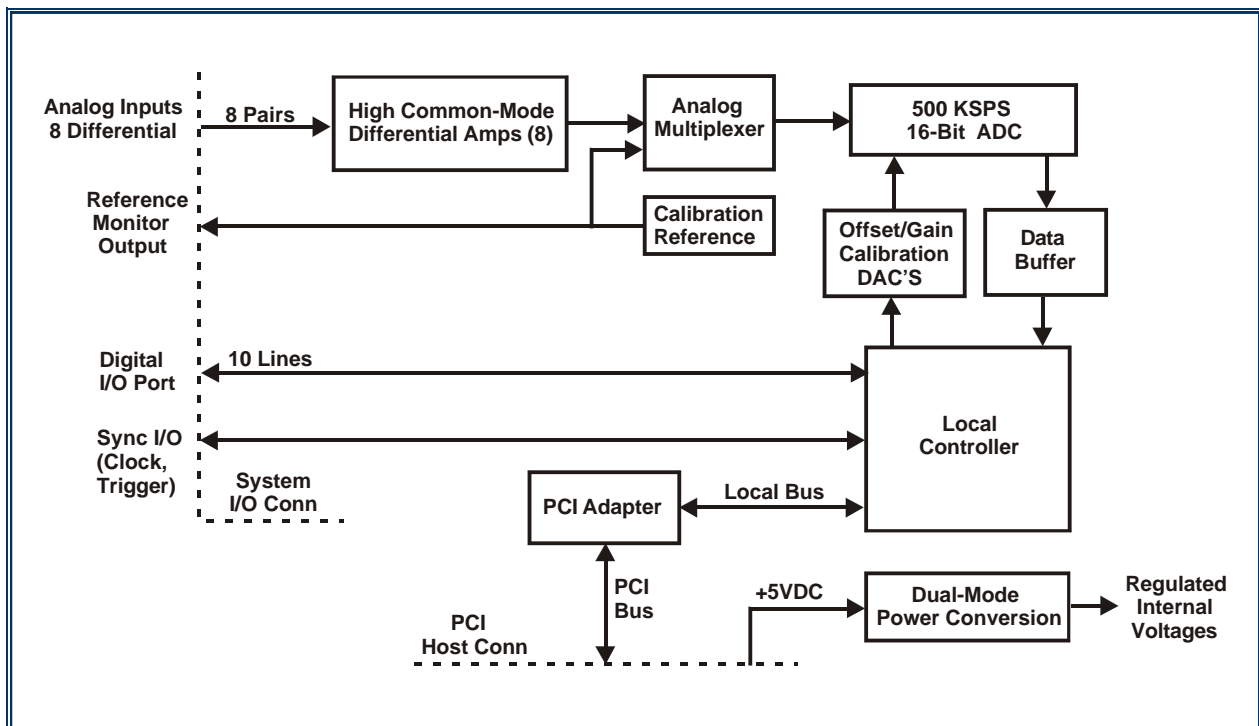


Figure 4.1-1. Functional Diagram

4.2 Control

A PCI interface adapter converts the control functions at the PCI interface into a local bus that is controlled in turn by a local controller. In addition to responding to host commands from the PCI interface adapter, the local controller performs all internal control operations for the module, including input scanning, data buffer access, digital I/O and autocalibration.

4.3 Electrical Power Conversion

Electrical power is obtained through the PCI interface as +5 VDC. To produce the various regulated power voltages that are required by the analog section of the module, the +5 VDC input is first converted by switching DC/DC converters into preregulated voltages that range from approximately +6 VDC to ± 17 VDC. These voltages then are postregulated to the final required output levels by series regulators that ensure very high-quality power rails.

4.4 Analog Functions

Each of eight differential analog input signals from the I/O connector passes through a differential amplifier that removes any common mode errors that might have been introduced by the external system. The eight amplifiers are divided into two groups of four amplifiers, with each group operating independently at one of two software-controlled High/Low ranges. An analog multiplexer scans the outputs of the differential amplifiers in a sequence that is established by a scan table in the local controller. The multiplexer also provides three subranges that are controlled by the scan table. The combined effect of the differential amplifier High/Low ranging and the multiplexer subranging provides overall input scaling from ± 2.5 Volts to ± 200 Volts fullscale.

A 16-bit A/D converter digitizes the output of the multiplexer into a series of 16-bit codes that are stored in a data buffer for subsequent extraction as measurement data through the PCI bus. Gain and offset errors inherent to the A/D converter are corrected during autocalibration by two 12-bit D/A converters.

Autocalibration is executed on-demand by the host, and performs a 12-bit successive-approximation sequence of corrections to both the gain and offset errors of the A/D converter. The final correction values are retained until the module is reset or power is removed. The calibration reference that is used during autocalibration is available for monitoring at a test pin in the system I/O connector.

4.5 External Clock and Trigger

Both the input sample clocking rate and the trigger rate of single-scan bursts are software controlled through internal dividers that operate from the module's master clock. The outputs from each of these dividers can be replaced with an external digital input, which then controls the associated clock or trigger function.

Digital clock and trigger outputs permit multiple modules to be clocked and scan-triggered simultaneously by connecting the clock and trigger outputs from one module to the clock and trigger inputs of another module. The number of modules that can be chained together in this manner is limited only by the availability of secure digital grounding between modules.

4.6 Digital Input/Output Port

The digital I/O port consists of eight bidirectional signals, one input-only signal, and one output-only signal. These digital signals are TTL compatible and use the host PCI bus ground as a digital return. All eight bidirectional signals are configured simultaneously as either inputs or outputs by the host, and are supported by a 256-byte FIFO buffer. The buffer is clocked from an internal rate generator, and can be used to generate continuous, one-shot, or periodic bit patterns.

PRELIMINARY

APPENDIX A
SUPPLEMENTARY MATERIAL



