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PMC-3311

**High-Speed 16-Channel
16-Bit PMC Analog Output Card**

REFERENCE MANUAL

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SECTION 1.0 OVERVIEW

1.1 Product Summary

The PMC-3311 is a single-width PCI mezzanine card (PMC) that provides access to sixteen precision analog output channels through a standard 32-Bit, 33MHz PCI bus interface. This product conforms to the mechanical and electrical requirements of the IEEE-1386 standard for common mezzanine cards, and complies with IEEE PCI local bus specification Revision 2.2.

Sixteen 16-Bit analog outputs can be clocked at rates to 1.0 MSPS (megasamples per second) per channel, for an aggregate throughput of 16 MSPS. Two output data buffers can be operated independently or synchronously, and four independent internal rate generators are available as clocking sources. The card can be supplied with fullscale output ranges of ± 2.5 , ± 5 or ± 10 Volts, and supports remote ground sensing for maximum accuracy at the loads.

A byte-wide bidirectional digital I/O port uses a 256-Byte FIFO buffer to support pattern generation and capture, or the port can be used for routine digital I/O functions.

Input connections from the system are accepted at the front panel through a standard 68-pin 0.05" subminiature-D male connector. Power requirements consist of a single +5 Volt source obtained from the PCI bus. Figure 1.1-1 shows the general locations of major functions and components.

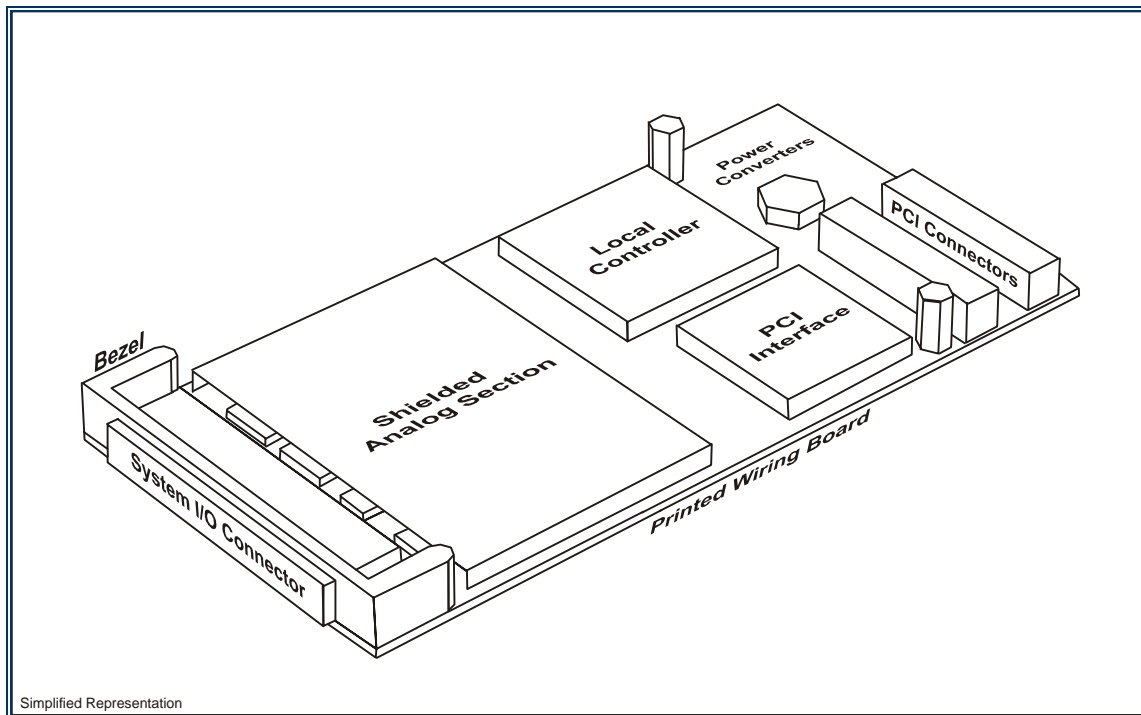


Figure 1.1-1. Physical Organization

1.2 Mechanical Outline

This product conforms to the mechanical constraints shown in Figure 1.2-1, in compliance with the IEEE-1386 standard for common mezzanine cards.

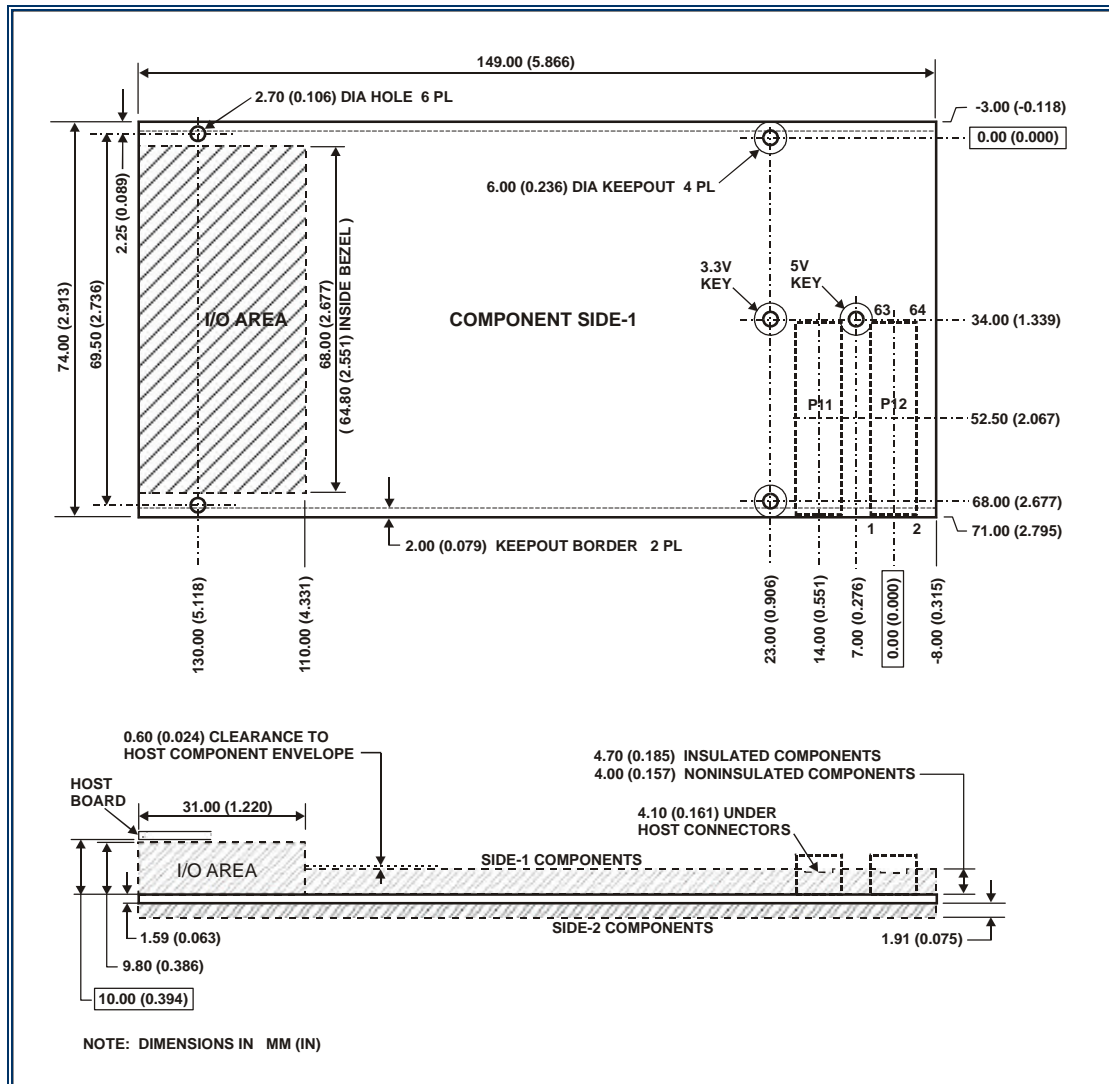


Figure 1.2-1. PMC Mechanical Detail

1.3 Document Scope

This reference manual describes the control characteristics and hardware installation requirements for the PMC-3311 card, and provides a functional description of internal hardware operation. Although occasional references are made to performance characteristics, the product specification SPEC-PMC3311 is the controlling document for performance parameters. An electrical schematic, if provided with this manual, represents the hardware configuration at the time of issue.

SECTION 2.0

CONTROL

2.1 Overview

The control interface for the PMC-3311 complies with the IEEE PCI local bus specification Revision 2.2 for a 32-bit data bus and a 33 MHz PCI clock. A PCI-9054 PLX™ PCI adapter provides communication between the PCI bus and the internal control bus. The module occupies 128 contiguous bytes of control space, and can be located on any 32-longword boundary in memory.

Local control registers, shown in Table 2.1-1, are accessed with single read or write operations, while three FIFO access registers support both single transactions and mastered DMA transactions. A single interrupt on the PCI INT-A line can respond to any of multiple selectable events. To ensure compatibility with subsequent firmware extensions, only zero-states should be written to control fields that are identified as "reserved."

The board control register (BCR) shown in Table 2.1-2 provides individual clearing functions for the three internal buffers, and gating functions for four rate generators. The BCR also controls the data coding format and provides a control bit for initializing the board. A single control bit initializes autocalibration.

2.2 Reset and Initialization

When a reset occurs on the PCI bus, both the PCI adapter and the local controller are initialized. The local controller autoloads configuration information from internal EPROM, and then initializes its internal registers to default values. The total time required for these operations is approximately 200-300 milliseconds. The PCI interrupt is disabled after a PCI reset occurs.

The local controller can be initialized without reconfiguring either the PCI adapter or the controller by setting the INITIALIZE control bit HIGH in the BCR. Local controller initialization requires approximately 30 milliseconds for execution, after which the control bit is cleared automatically and the local interrupt is asserted.

Upon completion of reset or initialization, the board is in the following state:

- ◆ All control registers are in their default states
- ◆ The initialization interrupt is selected and the local interrupt line is asserted
- ◆ All analog output channels are initialized to midrange (zero)
- ◆ All analog output and digital I/O clocking is disabled
- ◆ Analog output and digital I/O buffers are cleared (empty)
- ◆ Continuous sampling and simultaneous clocking are selected for both output buffers
- ◆ Digital bidirectional I/O lines are configured as Direct-I/O inputs
- ◆ Buffer A and B internal rate generators are adjusted to 720 kHz, and are disabled
- ◆ The trigger rate generator is adjusted to 360 kHz, and is disabled
- ◆ The digital I/O port clocking rate generator is adjusted to 18 MHz, and is disabled.

2.3 Analog Outputs

2.3.1 General Organization

Sixteen analog output channels are controlled through two independent FIFO output data buffers, Buffer-A and Buffer-B. Output Buffer-A controls all even-numbered output channels, and Buffer-B controls all odd-numbered output channels. This odd/even arrangement simplifies the migration of applications among boards that have varying numbers of resident channels. Individual output channels can be designated as either active or inactive.

Each output buffer can be clocked independently of the other buffer, or both buffers can be clocked synchronously. When clocking from a dedicated internal rate generator, the clocking rate for each buffer can be changed dynamically at specific points in an output function. Continuous and burst sampling modes are available, and the buffers can be operated independently in either looping or open configurations. The bidirectional digital I/O port also can be synchronized to analog output clocking.

2.3.2 Channel Selection

2.3.2.1 Enabling Mask

Each output channel is designated as either active or inactive through the Channel-Enable Mask register shown in Table 2.3.2-1. A channel is designated as **active** by setting the corresponding mask bit HIGH, or as **inactive** by clearing the bit LOW. During initialization, all channels are designated as active, and the outputs are initialized to midrange (zero). Only active channels are controlled through the output buffers. Each inactive channel retains either the initial midrange value or, if temporarily active after initialization, the last value received from a buffer.

Note: The default mask value of 0x0000 FFFF applies to all board configurations. For boards that have fewer than sixteen resident channels, mask bits corresponding to nonexistent channels have no effect and can be either cleared or left asserted after initialization.

2.3.2.2 Channel Scan

A **scan** is an output sequence that contains one complete set of active channels for the associated output buffer. A scan output sequence commences with the lowest-numbered active channel, and proceeds upward consecutively through the highest-numbered active channel.

2.3.3 Buffer Control

2.3.3.1 Data Registers

Each of the two analog output buffers is accessed through a dedicated FIFO register. Both registers support single-write accesses, or DMA accesses as DMA master. As illustrated in Tables 2.3.3.1-1 and 2.3.3.1-2, the two registers have identical functions. Each contains a data field (OUTPUT DATA), an END OF BURST control bit and a RATE CHANGE control bit. The two control bits are discussed in those sections that pertain to their specific functions.

2.3.3.1.1 Data Field

The analog OUTPUT DATA field is 16 bits long, and is right-justified to the LSB. Data bits above D15 are ignored.

2.3.3.1.2 Coding Formats

Analog output data can be coded either in offset binary format or in two's complement format (Figure 2.3.3.1-1). The default offset binary format is selected when the OFFSET BINARY DATA control bit in the BCR is HIGH. Clearing the control bit LOW selects two's complement format.

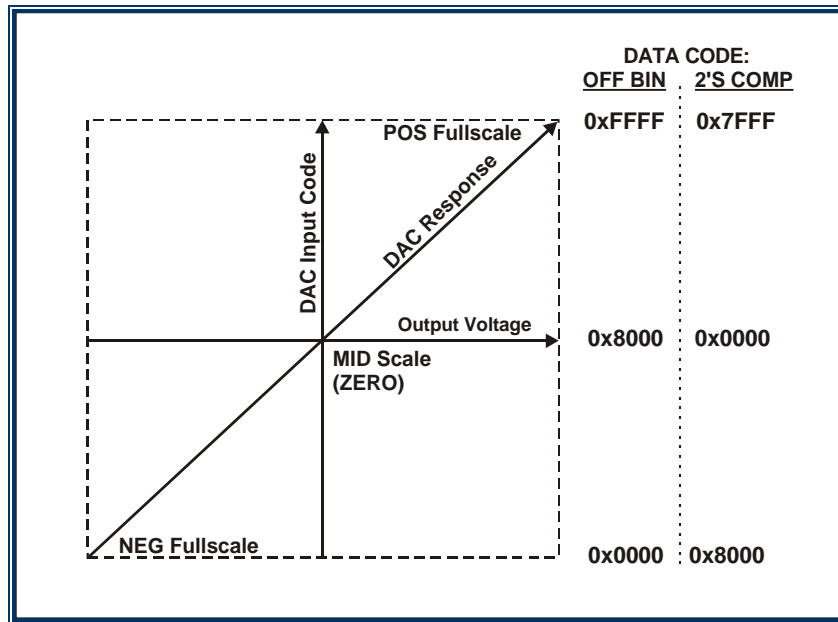


Figure 2.3.3.1-1. Analog Data Coding Formats

Note: Each block of data written to the buffer should contain an integral number of scans (Paragraph 2.3.2.2).

2.3.3.2 Control Registers

The operation of each analog output buffer is controlled through a dedicated register that controls clocking, burst triggering, and looping of the associated buffer, as well as buffer clearing. With the exceptions of clock and trigger controls, both buffer control registers have identical functions (Tables 2.3.3.2-1 and 2.3.3.2-2).

Each buffer can be cleared by asserting either the CLEAR BUFFER control bit in the associated buffer control register, or the associated CLEAR BUFFER control bit in the BCR. When a buffer is cleared, the buffer is emptied and any ongoing scan or burst operations are terminated.

2.3.3.3 Threshold Registers

Two threshold registers for each buffer provide a flag for controlling data flow from the PCIbus to the buffer. A HIGH and LOW threshold can be specified for each buffer, as shown in Table 2.3.3.3-1. Each threshold represents a specific number of output values in a buffer, and can be any integer value from zero up to the capacity of the buffer.

The two thresholds for each buffer control the status of the BUFFER THRESHOLD FLAG bit in the associated buffer control register. The BUFFER THRESHOLD FLAG is HIGH if the number of output values (samples) in the buffer is greater than the **low** threshold **and also** is less than or equal to the **high** threshold. The flag is LOW if the number of samples in the buffer is outside of the specified range.

An interrupt (Section 2.5) can be specified to occur on a HIGH-to-LOW transition of either threshold flag. This transition indicates that the number of samples in a buffer has moved outside of the specified range.

2.3.3.4 Physical Configuration

Each output buffer can be operated either in an open mode or in a looping mode. In the open mode, the buffer output is routed only to the output channels. In the looping, or closed, mode, the output of the buffer is connected to the input of the buffer, and data circulates within the buffer as well as being clocked to the analog outputs.

2.3.3.4.1 Open Buffer

When operating in the open mode, each output sample is flushed from the buffer as it is clocked to the associated analog output channel. The PCI bus has access to an open buffer, thereby permitting continuous streaming of data from the host to the analog outputs. The open mode is selected for a buffer when the LOOPING control bit is LOW in the associated buffer control register.

2.3.3.4.2 Looping (Closed) Buffer

Data within a looping buffer is retained indefinitely within the buffer, and external access from the PCI bus is inhibited. Data written to a looping buffer is discarded. Because data does not enter or leave a looping buffer, the number of samples in the buffer is constant after the looping mode has been selected. The looping mode is selected for a buffer by setting the LOOPING control bit HIGH in the associated buffer control register.

2.3.3.5 Buffer Clocking

A buffer responds to a clock input by transferring the current sample at the output of the buffer to the corresponding output channel, and by then advancing to the next sample in the buffer. If *sequential* clocking is selected (Section 2.3.3.7), the channel output updates immediately to the sample value that was transferred from the buffer. During simultaneous clocking, the outputs are updated only when the last sample in a scan (Section 2.3.2.2) is transferred from the buffer.

2.3.3.5.1 Clock Source Selection

Each output buffer can be clocked from a number of clock sources, as illustrated in Figure 2.3.3.5-1. Buffer-A can be clocked from a dedicated internal Rate-A Generator, or with a software clock, or from an external hardware clock input. The CLOCK SOURCE control field in the Buffer-A control register selects the Buffer-A clocking source.

A software clock is generated by asserting the SOFTWARE CLOCK control bit HIGH in the buffer control register, when the READY FOR CLOCK status bit is HIGH. The control bit clears automatically. The READY FOR CLOCK status bit is LOW while data is transferred from the buffer, and is HIGH when the buffer is ready to accept a new clock.

An external clock occurs at each HIGH-to-LOW transition of the external hardware clock input line at the system I/O connector.

Similarly, the CLOCK SOURCE field in the Buffer-B control register selects a dedicated RATE-B Generator, a software clock, or the external clock. Buffer-B also can be clocked from the Buffer-A clock source for synchronous operation.

To synchronize the digital I/O port with the analog output buffers, the digital port also can be clocked from the Buffer-A clock source.

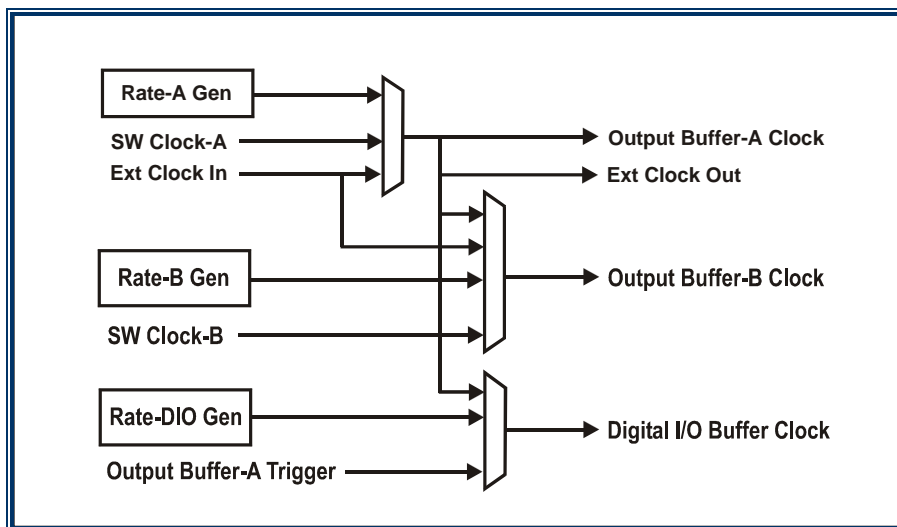


Figure 2.3.3.5-1. Rate Clock Organization

2.3.3.5.2 Enabling Clocking

The clocking of each buffer is enabled and disabled with the ENABLE BUFFER A/B CLOCKING control bits in the BCR. Regardless of which clock source is selected, actual clocking of the buffer will not commence until the corresponding ENABLE BUFFER A/B CLOCKING control bit is set HIGH.

Note: The ENABLE BUFFER A or B CLOCKING control bit should be LOW while buffer parameters are being configured, and then should be set HIGH to initiate buffer clocking.

2.3.3.5.3 Buffer Rate Generators

The frequency of a dedicated buffer rate generator is controlled up to 1.0MHz by the 16-bit RATE DIVISOR control field in the associated RATE-A or RATE-B control register (Tables 2.3.3.5-1 or 2.3.3.5-2). With a value **Nclk** in the register, the clocking frequency **Fclk** is:

$$\mathbf{Fclk} = 36,000 \cdot \mathbf{Nclk},$$

where **Fclk** is in kilohertz, and **Nclk** can be any integer from 36 to 65535. The clocking rate for the buffer in samples-per-second equals the generator frequency in Hertz.

2.3.3.5.4 Synchronous Clocking

Clocking of Buffer-A and Buffer-B can be synchronized by selecting the Buffer-A Clock option with the CLOCK SOURCE control field in the Buffer-B control register. In this configuration, Buffer-B clocks each time Buffer-A clocks, regardless of the source of the Buffer-A clock.

The digital I/O port (Section 2.5.4) also can be synchronized to the Buffer-A clock source.

2.3.3.5.5 Dynamic Rate Control

When an output buffer is operating from its dedicated rate generator, the frequency of the rate generator can be changed dynamically, or on the fly, at any point in an output function. The RATE CHANGE control bit in the buffer data register (Table 2.3.3.1-1 or 2.3.3.1-2), when HIGH, changes the context of the OUTPUT DATA field from "output data" to "rate-generator divisor."

If dynamic rate control is implemented, the rate-change occurs at the beginning of the scan for which the new rate is to be applied. The sample data values for the scan then follow the rate-change value. A rate-change value consists of the OUTPUT DATA field, and the RATE CHANGE control bit, which is asserted HIGH for the rate-change buffer value. The OUTPUT DATA field in the rate-change value replaces the **Nclk** divisor that is used to calculate the rate generator frequency **Fclk** in Section 2.3.3.5.3. The clocking rate changes to the new frequency when the scan in which it is inserted appears at the analog outputs. The values contained in the RATE-A and RATE-B control registers are unaffected by dynamic rate control operations.

Note: A Rate-Change data value should be inserted at the beginning of the scan (2.3.2.2) in which the new rate is to take effect.

The frequency of the rate generator can be changed repeatedly throughout an output function, and the last selected frequency will be retained until clocking is disabled or the board is initialized. When clocking is disabled, control of the rate generator is restored to the RATE-A and RATE-B control registers.

2.3.3.6 Sampling Modes

2.3.3.6.1 Continuous Sampling

In the *continuous sampling* mode, data flows through an output buffer to the analog outputs continuously as long as clocking is enabled and the buffer is not empty. The continuous sampling mode is selected for a buffer when the TRIGGER SOURCE field in the buffer control register is zero.

2.3.3.6.2 Triggered Bursts

The *burst sampling* mode permits the clocking of a buffer to be initiated and terminated at specified function boundaries. An example of this configuration is the generation of a complex transient waveform that occurs periodically with a low duty cycle. With continuous sampling, the buffered function would have to encompass the entire period of the transient, even though most of the samples might be zero or some other constant value. By using burst sampling however, only the transient waveform must be stored in the buffer.

A burst is initiated by a burst trigger, and is terminated by an END OF BURST (EOB) flag in the buffer data sequence. The trigger can originate from a number of sources, as described in Section 2.3.3.6.3, and the EOB flag is controlled through the output data buffer.

To identify the last sample in a sequence, the EOB control bit in the buffer data register is set HIGH in the data word that contains the last sample value in the burst. The burst then will terminate after the data sample that accompanies the EOB flag has been transferred to the associated analog output.

A buffer can contain multiple burst functions simultaneously. In this case, the bursts are executed sequentially, with each burst initiated by a trigger and terminated by an EOB flag.

2.3.3.6.3 Trigger Sources

Figure 2.3.3.6-1 illustrates the sources of burst triggering for the analog output data buffers. Buffer-A can be triggered from the Rate-TRIG Generator, or from a software trigger, or from an external hardware trigger. The software trigger is generated by asserting the SOFTWARE TRIGGER control bit HIGH in the Buffer-A control register when the READY FOR TRIGGER flag is HIGH. The control bit then clears automatically. The READY FOR TRIGGER flag is LOW during a burst, and is HIGH between bursts. Triggering is disabled if continuous operation is selected.

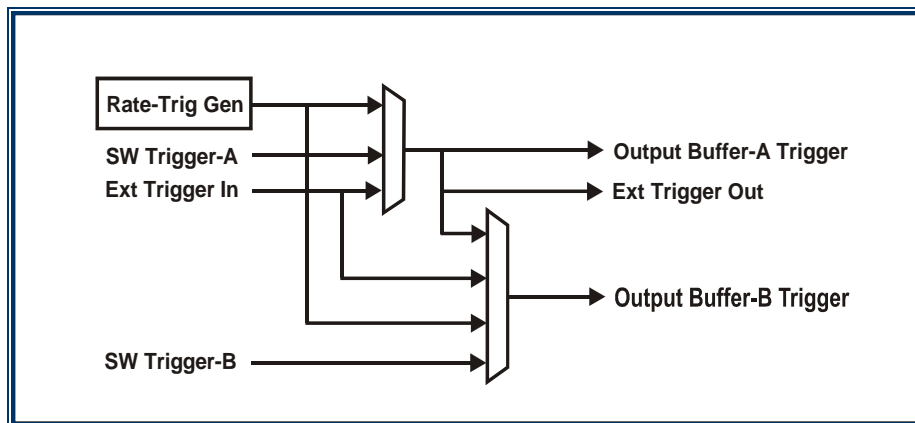


Figure 2.3.3.6-1. Burst Trigger Organization

When external triggering is selected, a trigger occurs on each HIGH-to-LOW transition of the external hardware *trigger input* at the system I/O connector. A LOW pulse is generated at the external hardware *trigger output* each time Buffer-A receives a trigger from any source.

Buffer-B also can be triggered from the Rate-Trig Generator, or from a software trigger, or from the external hardware trigger. Additionally, Buffer-B can be triggered from the Buffer-A trigger source, for synchronous burst operation.

As Figure 2.3.3.5-1 illustrates, the digital I/O port also can be clocked by the Buffer-A trigger. This feature can be used to generate external synchronizing patterns to accompany an analog output sequence.

2.3.3.6.4 Trigger Rate Generator

The Rate-Trig generator is controlled by the 20-bit RATE DIVISOR value in the Rate-Trig control register (Table 2.3.3.6-1). With a value **Ntrig** in the register, the triggering frequency **Ftrig** is:

$$\mathbf{Ftrig} = 36,000 \div \mathbf{Ntrig},$$

where **Ftrig** is in kilohertz, and **Ntrig** can be any integer from 36 to 1048575.

2.3.3.7 Clocking Modes

2.3.3.7.1 Simultaneous Clocking

The more common clocking mode is *simultaneous clocking*, in which all samples in a scan appear simultaneously at their corresponding outputs. The sample value for each channel in a scan is extracted from the buffer and stored in an intermediate register until the last sample in the scan is transferred from the buffer. When the last sample appears at the buffer output, all samples in the scan are transferred simultaneously to their respective outputs when a clock occurs.

Simultaneous clocking is selected when the SEQUENTIAL CLOCKING control bit is LOW in the associated buffer control register. ***In the simultaneous mode, clocking is suspended if a buffer becomes empty.*** Clocking resumes when additional data appears in the buffer.

NOTE: If clocking is suspended while operating in the simultaneous mode, data stored in the intermediate buffers may be retained and appear at the beginning of the next session. To prevent this from occurring, either ensure that all intermediate data has been clocked to the outputs, or initialize the board before commencing another clocking session.

2.3.3.7.2 Sequential Operation

When *sequential clocking* is selected, each sample in the buffer is clocked individually to the corresponding output, without regard to the sample's position in a scan. Scan boundaries have no effect during sequential clocking. For example, a series of five scans, each of which contains three active channels, would require 15 sample clocks to write all values to the outputs.

Sequential clocking is selected by setting the SEQUENTIAL CLOCKING control bit HIGH in the associated buffer control register.

2.3.3.8 Dynamic Function Replacement

Although access to a looping buffer is normally inhibited, a mechanism is provided to open the buffer temporarily to allow a new function to replace an existing function that is circulating within the buffer. Each buffer control register contains an ACCESS REQUEST control bit that, when asserted, serves as an interrupt request to the buffer sequencer.

When ACCESS REQUEST is asserted, the sequencer waits until the EOB flag in the existing (original) function appears at the output of the buffer, and then simultaneously asserts the BUFFER OPEN flag and opens the buffer. The original function then begins to be flushed from the buffer, which is now open and nonlooping, and the new function can now be loaded into the buffer. When the last sample of the original function is flushed from the buffer, as indicated by the second appearance of the EOB flag, the buffer closes automatically and further access is inhibited.

If loading of the new function is completed before the old function has been completely flushed from the buffer, the new function will commence seamlessly at the clock following the last value of the original function. If however, loading of the new function is not completed in time, the buffer will close and the new function will be truncated. DMA transfer rates therefore are of critical importance at high clocking rates, and a conservative transfer rate of 15-18 Megasamples per second from the host should be assumed.

2.3.4 Multicard Synchronization

If the external clock inputs and outputs are interconnected between multiple cards as described in Section 3.3, the output channels on all of the cards can be clocked synchronously. The first card in the daisy chain is designated as the *initiator card*, and provides the clock signal for all of the other cards in the chain, designated as *target cards*. All target cards have External Hardware Clock selected in the CLOCK SOURCE field of their buffer control registers, and the initiator can be configured for any available clock source. When configured in this manner, the outputs of all target cards will clock synchronously with the Buffer-A clock on the initiator.

Similarly, by daisy-chaining the trigger inputs and outputs between the cards, all target cards can be burst-synchronized to the initiator card. The target cards will have External Hardware Trigger selected in the TRIGGER SOURCE fields of their buffer control registers, and the initiator card can be triggered from any available trigger source. All target cards then will initiate a burst each time Buffer-A on the initiator card receives a trigger.

2.3.5 Remote Ground Sensing

The analog outputs can be operated in a pseudo-differential mode by connecting the remote sense pin in the system I/O connector to a remote ground that is common to all output loads. To take advantage of this connection, the REMOTE SENSE control bit must be set HIGH in the BCR. To prevent extraneous interference from being introduced through the remote-sense line, the REMOTE SENSE control bit should be left in the default LOW state unless the system application specifically requires remote ground sensing.

2.4 Digital Input/Output

2.4.1 Digital I/O Control Register

System digital I/O signals are controlled through the Digital I/O control register shown in Table 2.4.1-1. A single external output line follows the DIG AUX 01 OUTPUT control bit, and the DIG AUX 00 INPUT status bit follows a single external input line. Status bits D08-D11 are read-only flags that indicate the extent to which the digital I/O buffer is filled.

2.4.2 Bidirectional Digital Buffer

Eight bidirectional lines provide a byte-wide data FIFO port that is accessed through the Digital I/O Buffer register listed in Table 2.4.2-1. Bits D00-D07 of the buffer correspond to external digital I/O lines DIG IO 00-07 respectively, with no logic inversions. The buffer supports both single-read/write and mastered DMA transactions. Clocking of the buffer is enabled by setting the ENABLE CLOCKING control bit HIGH in the digital I/O control register. If the DIRECT I/O control bit in the digital I/O control register is HIGH, bidirectional digital I/O data bypasses the digital I/O FIFO, and the clocking input is ignored.

The digital I/O buffer is organized as an 8-bit by 256-byte FIFO, the direction of which is determined by the state of the DATA DIRECTION OUT control bit in the digital I/O control register. If the DATA DIRECTION OUT control bit is LOW, external lines DIG IO 00-07 are configured as inputs. In this case, the input of the FIFO accepts input data from the external lines DIG IO 00-07, and the FIFO output is available to the PCI bus. The BUFFER LOOP control bit in the digital I/O control register has no effect while the external bidirectional lines are configured as inputs.

If the DATA DIRECTION OUT control bit is HIGH, external lines DIG IO 00-07 become digital outputs, and the FIFO output is available to external lines DIG IO 00-07. If the DIRECT I/O control bit in the digital I/O control register is LOW, the input of the FIFO accepts data from the PCI bus. If the BUFFER LOOP control bit in the digital I/O control register is HIGH while the port is configured as an output port, data already present in the FIFO recirculates within the FIFO, and write transactions from the PCIbus are ignored.

NOTE: The output of the digital I/O FIFO retains either (a) the first value written to the FIFO after the FIFO is cleared, or (b) the last value read from the FIFO. Clearing the FIFO does not remove the output value, and least one clock is required to fetch a new value.

Table 2.4.2-2 summarizes the behavior of the byte-wide digital I/O port in its various operating modes. Table 2.4.2-3 lists two simple examples of typical operating sequences.

2.4.3 Digital I/O Clocking

The CLOCK SOURCE field permits the digital I/O port to be clocked either from an independent internal rate generator, or to be synchronized to the Buffer-A clocking or trigger source. If the Rate-DIO generator is selected, the port is clocked from the dedicated Rate-DIO Generator.

When Buffer-A Clock Source is selected, the digital I/O port receives a single clock each time Buffer-A is clocked (Figure 2.3.4.3-1). If Buffer-A Trigger Source is selected, the digital I/O port clocks each time Buffer-A receives a trigger.

When the bidirectional digital I/O lines are configured as an output port, data from the digital I/O buffer is clocked to the system I/O connector. If the bidirectional I/O lines are configured as an input port, data from the I/O lines is clocked into the digital I/O buffer at the rate determined by the digital I/O port clock source.

2.4.4 Rate-DIO Rate Generator

This generator is controlled by the 20-bit Digital Rate Gen control register shown in Table 2.4.4-1. With a value **Ndig** in the register, the digital I/O buffer clocking rate **Fdig** is:

$$\mathbf{Fdig} = 36 \cdot \mathbf{Ndig},$$

where **Fdig** is in megahertz, and **Ndig** can be any integer from 2 to 1048575.

NOTE: The ENABLE RATE-DIO GENERATOR control bit in the BCR must be HIGH in order to enable clocking from the Rate-DIO generator.

2.5 Interrupts

Specific events occurring within the module can be selected to produce an interrupt request on the single PCI interrupt line (INT-A). For the interrupt to be active however, it must first be enabled through the PCI adapter.

To enable interrupts from the PCI adapter:

- a. Determine the configuration address of the runtime interrupt status control register:
 - ◆ Read the PCI base address in PCI configuration space. The offset for the base address is 0x10 for memory-mapped configurations, or 0x14 for I/O-mapped configurations.
 - ◆ Add 0x68 to the base address to obtain the address of the interrupt status control register.
- b. Read the interrupt status control register, and write the value back to the register after logically OR'ing the pattern 0x0000 0900 to the value.

2.5.1 Organization

Interrupt control fields in the Interrupt Control register (Table 2.5-1) are organized into a selection field and a response field. Each available interrupt event has both a selection control bit and a corresponding response status bit. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, by clearing either the response bit or the associated selection bit.

NOTE: The interrupt response status bits can only be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The PCI interrupt output from the module is asserted if any response bit in the interrupt control register is asserted (and if the interrupt is enabled in the PCI adapter). To clear the interrupt, all response bits must be cleared.

2.5.2 Event Detection

Interrupt event detection is edge-activated on a transition of the selected event from false to true. Once asserted, each response status bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

2.6 Direct Memory Access

For those registers that support DMA, PCI data transfers are executed with the module acting as DMA master. The typical local configuration registers listed in Table 2.6-1 control the DMA configuration for data transfers both to and from the module.

2.7 Autocalibration

To ensure full conformance with the product specification, autocalibration should always be invoked at least once after power has been applied to the board, or after a software or hardware reset has occurred. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs immediately after power is applied.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration, which has a duration of approximately 4-8 seconds, is indicated by the AUTOCAL bit clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event. Read/write accesses from the PCI bus during autocalibration can produce unpredictable results, and are not recommended. The software-controlled board configuration that exists when autocalibration is invoked is restored when autocalibration has been completed.

The autocalibration process may be unable to successfully calibrate all analog channels if a board is marginal or defective. Should this situation occur, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS after autocalibration indicates that the calibration was successful.

NOTE: Accesses to the board while autocalibration is in progress should be restricted to read-only transactions from the board control register (BCR) and the Interrupt Control register.

2.8 Control Sequence Examples

This section provides general descriptions of typical control sequences for producing the following operating modes. These examples represent only a few of many possible applications:

Direct Output; Sequential mode:	Data written to the buffer is clocked immediately to the outputs.
Continuous Function, Nonlooping:	Streaming mode. Data flows through the buffer to the outputs.
Continuous Function, Looping:	Periodic Continuous Function. The function is retained in the buffer, and is clocked continuously to the outputs..
Burst Function, Looping:	Periodic One-Shot function. Clocking is initiated by a trigger, after which the function is clocked to the outputs and then terminates until another trigger occurs. The function remains in the buffer, and can be triggered repeatedly.
Dynamic Function Replacement:	An currently clocking function in a looping (closed) buffer is replaced seamlessly by a new function.

Each example can be applied to either buffer, and assumes that the following parameters have already been selected:

Parameter	Reference Section
Active Channels	2.3.2
Buffer Threshold; if required	2.3.3.3
Clock Source	2.3.3.5.1
Clocking Rate: (If a rate generator is the selected clocking source)	2.3.3.5.3
Clocking Mode; Simultaneous or Sequential	2.3.3.7

2.8.1 Direct Output

- a. Select sequential clocking.
- b. Enable clocking and write a sequence of sample values to the buffer (2.3.3.1). Each sample appears individually at its associated output when a clock occurs.

2.8.2 Continuous Function, Nonlooping

This operating mode is similar to the Direct Output mode, but the buffer is not allowed to become empty, and the output is a continuous sequence of sample values.

- a. Write an initial block of output values to the buffer (2.3.3.1). The block should contain an integral number of scans (2.3.2.2).
- b. Enable clocking (2.3.3.5.2).
- c. Commence writing a sequence of output values to the buffer (2.3.3.1). Using the buffer threshold flag (2.3.3.3), ensure that the buffer becomes neither empty nor full.
- d. The active outputs receive new values from the buffer continuously until the input data stream to the buffer terminates. When data input from the PCIbus ceases, the output values remaining in the buffer continue to be clocked to the outputs until the buffer becomes empty.

2.8.3 Continuous Function, Looping

- a. Write an entire function or sequence of output values to the buffer (2.3.3.1).
- b. Select the looping mode (2.3.3.4.2). Subsequent values written to the buffer are ignored.
- c. Enable clocking (2.3.3.5.2).
- d. The active outputs receive new values from the buffer continuously until clocking is disabled. The function is retained indefinitely, and circulates continuously within the buffer.

2.8.4 Burst Function, Looping

- a. Write an entire function or sequence of values to the buffer (2.3.3.1). Attach the END OF BURST flag to the last value in the function (2.3.3.6.2).
- b. Select the looping mode (2.3.3.4.2). Subsequent values written to the buffer are ignored.
- c. Select a burst triggering source (2.3.3.6.3). Selection of a burst trigger source automatically enables the burst sampling mode.
- d. Select the trigger rate if the trigger source is a rate generator (2.3.3.6.4).
- e. Enable clocking (2.3.3.5.2).
- f. Clocking commences when the first trigger occurs, and terminates when the last value in the function has been clocked to the outputs. The function is retained indefinitely within the buffer, and each subsequent trigger initiates the function again.

2.8.5 Dynamic Function Replacement

- a. Initiate a continuous looping function, as described above in 2.8.3, but attach an END OF BURST tag (Buffer bit D16) to the last value in the function.

Note: Do not select a burst triggering mode. The EOB tag is used here only to identify the end of the function.

- b. Set the ACCESS REQUEST flag HIGH in the buffer control register, and wait for the BUFFER OPEN flag to be asserted HIGH.
- c. Load a new function into the buffer *while the BUFFER-OPEN flag is HIGH*. (The flag will go LOW again when the last value of the original function is clocked from the buffer). Attach an EOB flag to the last value of the new function.

Note: Do not clear the ACCESS REQUEST flag, or the buffer may close prematurely. The request flag is cleared automatically when the last value of the original function is clocked from the buffer.

- d. The remainder of the original function clocks to the outputs, after which the buffer closes and the new function seamlessly begins clocking to the outputs and circulating within the buffer.

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2.8 Control Section Tables

Table 2.1-1 Local Control Registers

LOCAL ADDR	ACCESS MODE	REGISTER	DEFAULT	FUNCTION
0x00	RW	BOARD CONTROL	0x0002 0001	Board Control Register (BCR)
0x04	RW	CHANNEL-ENABLE MASK	0x0000 FFFF	Enabling mask for output channels
0x08	WO (DMA)	OUTPUT BUFFER-A DATA	---	Buffer-A output data
0x0C	RW	BUFFER-A HIGH THRESHOLD	0x0000 3FF0	Buffer-A status flag high threshold
0x10	RW	BUFFER-A LOW THRESHOLD	0x0000 0000	Buffer-A status-flag low threshold
0x14	RW	BUFFER-A CONTROL	0x0000 0401	Buffer-A control register
0x18	WO (DMA)	OUTPUT BUFFER-B DATA	---	Buffer-B output data
0x1C	RW	BUFFER-B HIGH THRESHOLD	0x0000 3FF0	Buffer-B status flag high threshold
0x20	RW	BUFFER-B LOW THRESHOLD	0x0000 0000	Buffer-B status-flag low threshold
0x24	RW	BUFFER-B CONTROL	0x0000 0401	Buffer-B control register
0x28	RW (DMA)	DIGITAL I/O BUFFER	0x0000 00XX	Bidirectional digital I/O data FIFO buffer
0x2C	R/W	DIGITAL I/O CONTROL	0x0000 0110	Digital I/O control register
0x30	R/W	RATE-A CONTROL	0x0000 0032	Buffer-A rate generator divider
0x34	R/W	RATE-B CONTROL	0x0000 0032	Buffer-B rate generator divider
0x38	R/W	RATE-TRIG CONTROL	0x0000 0064	Burst-Trigger rate generator divider
0x3C	R/W	RATE-DIO CONTROL	0x0000 0002	Digital I/O rate generator divider
0x40	RW	INTERRUPT CONTROL	0x0000 0101	Interrupt event selection and status
0x44	RO	F/W Revision *	---	*
0x48	RO	Autocal Values *	---	*
0x4C-0x7F	RO	(Reserved)	---	(Inactive)

RW = Read/Write; RO = Read-Only; WO = Write-Only; X = Undefined state.

* Test registers; shown for reference only.

Table 2.1-2. Board Control Register; Offset 0x00; Default 0x0002 0001

DATA BIT	DESIGNATION	DEFAULT	DESCRIPTION
D00	OFFSET BINARY DATA	1	Selects two's complement output data format when LOW, or offset binary format when HIGH.
D01 *	BUFFER-A THRESHOLD FLAG	0	Asserted HIGH when the number of values in Buffer-A is greater than the Buffer-A LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the Buffer-A control register.
D02 *	BUFFER-B THRESHOLD FLAG	0	Asserted HIGH when the number of values in Buffer-B is greater than the Buffer-B LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the Buffer-B control register.
D03	(Reserved)	0	---
D04 **	CLEAR BUFFER-A	0	Clears output Buffer-A and sequencer
D05 **	CLEAR BUFFER-B	0	Clears output Buffer-B and sequencer
D06 **	CLEAR DIGITAL I/O BUFFER	0	Clears the digital I/O buffer and sequencer
D07	(Reserved)	0	---
D08	ENABLE RATE-A GENERATOR	0	Enables operation of the Rate-A Generator
D09	ENABLE RATE-B GENERATOR	0	Enables operation of the Rate-B Generator
D10	ENABLE RATE-TRIG GENERATOR	0	Enables operation of the Rate-Trig Generator
D11	ENABLE RATE-DIO GENERATOR	0	Enables operation of the Rate-DIO Generator
D12	ENABLE BUFFER-A CLOCKING	0	Enables Buffer-A clocking when HIGH
D13	ENABLE BUFFER-B CLOCKING	0	Enables Buffer-B clocking when HIGH
D14-15	(Reserved)	0	---
D16 **	AUTOCAL	0	Initiates an autocalibration operation when asserted.
D17 *	AUTOCAL PASS	1	Indicates a successful autocalibration when HIGH, or an autocalibration failure when LOW.
D18	REMOTE SENSE	0	Enables remote ground sensing
D19 **	INITIALIZE BOARD	0	Initializes the board when asserted. Sets all defaults.
D20-31 *	(Reserved)	0x0	Read-only. Returns all-zero value.

* Read-Only. All other bits are Read/Write. ** Control bit clears automatically upon completion.

Table 2.3.2-1. Channel-Enable Mask Register; Offset 0x04; Default 0x0000 FFFF

DATA BIT	DESIGNATION	DEF	DESCRIPTION
D00	ENABLE CHANNEL 00	1	Buffer-A channel-enable mask. A channel is enabled if the associated mask bit is HIGH, or is disabled if the bit is LOW.
D01	ENABLE CHANNEL 02	1	
D02	ENABLE CHANNEL 04	1	
D03	ENABLE CHANNEL 06	1	
D04	ENABLE CHANNEL 08	1	
D05	ENABLE CHANNEL 10	1	
D06	ENABLE CHANNEL 12	1	
D07	ENABLE CHANNEL 14	1	
D08	ENABLE CHANNEL 01	1	Buffer-B channel-enable mask
D09	ENABLE CHANNEL 03	1	
D10	ENABLE CHANNEL 05	1	
D11	ENABLE CHANNEL 07	1	
D12	ENABLE CHANNEL 09	1	
D13	ENABLE CHANNEL 11	1	
D14	ENABLE CHANNEL 13	1	
D15	ENABLE CHANNEL 15	1	
D16-31 *	(Reserved)	0	Read-only. Returns all-zero value.

* Read-only. All other control bits are read/write.

Table 2.3.3.1-1. Output Buffer-A Data Register; Offset: 0x08

DATA BIT	DESIGNATION	FUNCTION
D00-15	OUTPUT DATA	16-bit analog output data
D16	END OF BURST (EOB)	EOB: Indicates the end of a burst function. Principal purpose is the termination of a burst.
D17	RATE CHANGE	New Clocking Rate-A: The OUTPUT DATA field replaces the Rate Control-A register for frequency control.
D18-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.3.1-2. Output Buffer-B Data Register; Offset: 0x18

DATA BIT	DESIGNATION	FUNCTION
D00-15	OUTPUT DATA	16-bit analog output data
D16	END OF BURST (EOB)	EOB: Indicates the end of a burst function. Principal purpose is the termination of a burst.
D17	RATE CHANGE	New Clocking Rate-B: The OUTPUT DATA field replaces the Rate Control-B register for frequency control.
D18-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.3.2-1. Buffer-A Control Register;

Offset: 0x14; Default: 0x0000 0401

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-01	R/W	CLOCK SOURCE	1	Selects and enables the Buffer-A clocking source: Code Buffer-A Clocking Source ----- ----- 0 Software Clocking Enabled 1 Rate-A Generator 2 External Hardware Clock 3 (Reserved)
D02	RO	READY FOR CLOCK	0	When HIGH, indicates that a software clock will be accepted by Buffer-A if software clocking is enabled.
D03	R/W	* SOFTWARE CLOCK	0	Produces a single Buffer-A clock when asserted, if software clocking is enabled and READY FOR CLOCK is HIGH.
D04-05	R/W	TRIGGER SOURCE	0	Selects and enables the Buffer-A burst trigger source: Code Buffer-A Burst Trigger Source ----- ----- 0 Continuous Operation. Trigger Disabled 1 Rate-Trig Generator 2 External Hardware Trigger 3 (Reserved)
D06	RO	READY FOR TRIGGER	0	When HIGH, indicates that a Buffer-A software trigger will be accepted if software triggering is enabled.
D07	R/W	* SOFTWARE TRIGGER	0	Produces a single Buffer-A trigger when asserted, if triggering is enabled and READY FOR TRIGGER is HIGH. Active in all triggering modes except Continuous Operation.
D08	R/W	LOOPING	0	When HIGH, selects Buffer-A looping. Disables PCIbus access to the buffer unless ACCESS REQUEST is asserted.
D09	R/W	* ACCESS REQUEST	0	Requests access to a looping (closed) Buffer-A when HIGH. Accessibility is indicated by the BUFFER OPEN flag.
D10	RO	BUFFER OPEN	1	When HIGH, indicates that Buffer-A will accept data.
D11	R/W	* CLEAR BUFFER	0	Resets Buffer-A to empty. Duplicated in the BCR.
D12	R/W	SEQUENTIAL CLOCKING	0	Selects sequential clocking for Buffer-A when HIGH, or simultaneous clocking when LOW.
D13	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in Buffer-A is greater than the Buffer-A LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the board control register (BCR).
D14-31	RO	(Reserved)	0	Read-only. Returns all-zero value.

R/W = Read/Write, RO = Read-only.

* Clears LOW automatically when operation is completed.

Table 2.3.3.2-2. Buffer-B Control Register; Offset: 0x24; Default: 0x0000 0401

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-01	R/W	CLOCK SOURCE	1	Selects and enables the Buffer-B clocking source: Code Buffer-B Clocking Source ----- ----- 0 Software Clocking Enabled 1 Rate-B Generator 2 External Hardware Clock 3 Buffer-A Clock Source
D02	RO	READY FOR CLOCK	0	When HIGH, indicates that a software clock will be accepted by buffer-B if software clocking is enabled.
D03	R/W	* SOFTWARE CLOCK	0	Produces a single Buffer-B clock when asserted, if software clocking is enabled and READY FOR CLOCK is HIGH.
D04-05	R/W	TRIGGER SOURCE	0	Selects and enables the Buffer-B burst trigger source: Code Buffer-B Burst Trigger Source ----- ----- 0 Continuous Operation. Trigger Disabled 1 Rate-Trig Generator 2 External Hardware Trigger 3 Buffer-A Trigger Source
D06	RO	READY FOR TRIGGER	0	When HIGH, indicates that a Buffer-B software trigger will be accepted if software triggering is enabled.
D07	R/W	* SOFTWARE TRIGGER	0	Produces a single Buffer-B trigger when asserted, if triggering is enabled and READY FOR TRIGGER is HIGH. Active in all triggering modes except Continuous Operation.
D08	R/W	LOOPING	0	When HIGH, selects Buffer-B looping. Disables PCIbus access to the buffer unless ACCESS REQUEST is asserted.
D09	R/W	* ACCESS REQUEST	0	Requests access to a looping (closed) Buffer-B when HIGH. Accessibility is indicated by the BUFFER OPEN flag.
D10	RO	BUFFER OPEN	1	When HIGH, indicates that Buffer-B will accept data.
D11	R/W	* CLEAR BUFFER	0	Resets Buffer-B to empty. Duplicated in the BCR.
D12	R/W	SEQUENTIAL CLOCKING	0	Selects sequential clocking for Buffer-B when HIGH, or simultaneous clocking when LOW.
D13	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in Buffer-B is greater than the Buffer-B LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the board control register (BCR).
D14-31	RO	(Reserved)	0	Read-only. Returns all-zero value.

R/W = Read/Write, RO = Read-only.

* Clears LOW automatically when operation is completed.

Table 2.3.3.3-1. Output Buffer Threshold Registers ;

HIGH Thresholds: Offsets: Buffer-A: 0x0C, Buffer-B: 0x1C; Default: 0x0000 3FF0;

LOW Thresholds: Offsets: Buffer-A: 0x10, Buffer-B: 0x20; Default: 0x0000 0000;

DATA BIT	DESIGNATION	FUNCTION
D00-15	BUFFER THRESHOLD	16-Bit buffer HIGH or LOW threshold value. The associated buffer threshold flag is asserted HIGH when buffer contents are greater than the LOW threshold, and less than or equal to the HIGH threshold.
D16-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.3.5-1. Rate-A Control Register; Offset: 0x30; Default: 0x0000 0032 *

DATA BIT	DESIGNATION	FUNCTION
D00-15	RATE DIVISOR	Rate generator divisor for master clock
D16-31	(Reserved)	Read-only. Returns all-zero value.

* The Rate-A generator frequency can be controlled also through output data Buffer-A.

Table 2.3.3.5-2. Rate-B Control Register; Offset: 0x34; Default: 0x0000 0032 *

DATA BIT	DESIGNATION	FUNCTION
D00-15	RATE DIVISOR	Rate generator divisor for master clock
D16-31	(Reserved)	Read-only. Returns all-zero value.

* The Rate-B generator frequency can be controlled also through output data Buffer-B.

Table 2.3.3.6-1. Rate-Trig Control Register; Offset: 0x38; Default: 0x0000 0064

DATA BIT	DESIGNATION	FUNCTION
D00-19	RATE DIVISOR	Rate generator divisor for master clock
D20-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.4.1-1. Digital I/O Control Register; Offset 0x2C; Default 0x0000 0110

BITS	DESIGNATION	DEFAULT	FUNCTION *
D00	DATA DIRECTION OUT	0	Configures the bidirectional data lines as outputs from D00-07 of this register when asserted HIGH, or as inputs to this register when LOW.
D01	BUFFER LOOP	0	Closes the buffer for data recirculation when HIGH, opens the buffer for pass-thru operation when LOW.
D02	CLEAR DIGITAL BUFFER	0	Clears the digital I/O buffer. (Bit clears automatically). Duplicated in the BCR.
D03	ENABLE CLOCKING	0	Enables digital I/O buffer clocking from Rate Generator-D
D04	DIRECT I/O	1	Routes I/O data around (bypasses) the digital I/O FIFO
D05	(Reserved)	---	---
D06	DIG AUX 01 OUTPUT	0	Output-only digital line
D07	DIG AUX 00 INPUT	0	Read-Only. Input-only digital line
D08	BUFFER EMPTY	1	Read-Only. HIGH only when the digital buffer is empty.
D09	BUFFER 1/4 FULL	0	Read-Only. HIGH when the buffer is 1/4 full or more.
D10	BUFFER 3/4 FULL	0	Read-Only. HIGH when the buffer is 3/4 full or more.
D11	BUFFER FULL	0	Read-Only. HIGH only when the buffer is full.
D12-13	CLOCK SOURCE	0	Selects and enables the Digital I/O port clocking source: Code Digital I/O Clocking Source ----- ----- 0 Rate-DIO Generator 1 Buffer-A Clock Source 2 Buffer-A Trigger Source 3 (Reserved)
D14-31	(Reserved)	---	Read-only. Returns all-zero value.

* All control bits are READ/WRITE unless indicated otherwise

Table 2.4.2-1. Digital I/O Buffer Register; Offset: 0x28

DATA BIT	DESIGNATION	FUNCTION
D00-07	DIGITAL I/O DATA	Bidirectional digital I/O data FIFO
D08-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.4.2-2. Digital I/O Buffer Activity Modes

DATA DIRECTION	PCibus TRANSACTION	BUFFER LOOP	DIRECT I/O	DATA ACTIVITY
INPUT	READ	Don't Care	LOW	PCibus reads the digital I/O FIFO.
INPUT	READ	Don't Care	HIGH	DIRECT-READ MODE: (Default) PCibus reads directly from the external digital I/O lines
INPUT	WRITE	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus data is ignored.
OUTPUT	WRITE	Don't Care	HIGH	DIRECT-WRITE MODE: PCibus writes directly to the external digital I/O lines.
OUTPUT	WRITE	LOW	LOW	PASSTHRU MODE: PCibus writes to the digital I/O FIFO. External digital I/O lines follow the FIFO output.
OUTPUT	WRITE	HIGH	LOW	RECIRCULATION MODE (Looping): PCibus data is ignored. Data already present in the FIFO recirculates. External digital I/O lines follow the FIFO output.
OUTPUT	READ	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus reads the previous value written to the port.

Table 2.4.2-3. Typical Digital I/O Operation

CLOCKED OUTPUT PORT		CLOCKED INPUT PORT	
STEP	OPERATION	STEP	OPERATION
1 *	Configure as an output port. (DATA DIRECTION OUT = HIGH) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)	1 *	Configure as an input port. (DATA DIRECTION OUT = LOW) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)
2	Load the buffer with a pattern sequence.	2	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)
3	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)	3	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)
4	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)	4	The buffer begins to fill with data from the digital I/O port.
5	Data from the buffer begins to clock to the digital I/O port. If looping has not been selected, the buffer accepts subsequent data from the PCI bus.		

* Adjust all digital I/O control register bits simultaneously.

** Do not clear the buffer again at this point. For looping (periodic function generation), set BUFFER LOOP = HIGH.

Table 2.4.4-1. Rate-DIO Control Register; Offset: 0x3C; Default: 0x0000 0002

Offset: 0x3C;

Default: 0x0000

DATA BIT	DESIGNATION	FUNCTION
D00-19	RATE DIVISOR	Rate generator divisor for master clock
D20-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.5-1 Interrupt Control Register; Offset 0x40; Default 0x0000 0101

CONTROL BITS	INTERRUPT EVENT	FUNCTION
D00	Initialization completed	Interrupt event selection. Enables assertion of the corresponding event flag (below) when the selected event occurs.
D01	Autocal completed	
D02	Buffer-A threshold flag HIGH-to-LOW transition	
D03	Buffer-B threshold flag HIGH-to-LOW transition	
D04	(Reserved)	
D05	(Reserved)	
D06	Digital buffer 1/4-Full HIGH-to-LOW transition	
D07	Digital buffer 3/4-Full LOW-to-HIGH transition	
D08	Initialization completed	Interrupt response. Asserted HIGH when a selected interrupt (above) occurs. Remains HIGH until cleared LOW. The PCI bus INT A interrupt is asserted while any event flag in this register is asserted..
D09	Autocal completed	
D10	Buffer-A threshold flag HIGH-to-LOW transition	
D11	Buffer-B threshold flag HIGH-to-LOW transition	
D12	(Reserved)	
D13	(Reserved)	
D14	Digital buffer 1/4-Full HIGH-to-LOW transition	
D15	Digital buffer 3/4-Full LOW-to-HIGH transition	
D16-31	(Reserved)	

Table 2.6-1. Typical DMA Control Registers

CONFIGURATION REGISTER	OFFSET*	DMA FUNCTION	COMMENTS and TYPICAL VALUES
PCI Status and Command	0x04	Bus mastering selection.	Logically OR 0x0004 for bus mastering.
DMA-0 Mode	0x80	32-Bit bus, Interrupt on done, nonincrementing, local bursting, DMA Chan-0	0x0002 0D43
DMA-0 PCI Address	0x84	Initial PCI data address	Application-dependent
DMA-0 Local Address	0x88	Initial local address	Local address of data register (Table 2.1-1)
DMA -0 Transfer Byte Count	0x8C	Number of bytes in transfer	Application-dependent
DMA Descriptor Counter	0x90	Transfer direction	0x0000 0000, PCI to card (write) 0x0000 000A, Card to PCI (read)
DMA-0 Command Status	0xA8	Enable/initiate transfer	0x0000 0001 to enable transfer 0x0000 0003 to initiate transfer

* From base address.

SECTION 3.0 HARDWARE INSTALLATION

3.1 System Configuration

A typical installation of a PMC I/O module involves several fundamental tasks, namely:

- ◆ Configuration of the PMC module
- ◆ System cabling and connections
- ◆ Physical installation of the PMC module on the PMC host board
- ◆ Maintenance.

The configuration of the PMC-3311 is established at the factory, and no electrical modifications are required in the field. This section provides specific information and guidelines pertaining to the remaining installation tasks. Contact Sales at Rymic Systems if prewired or custom cable assemblies are required.

3.1.1 I/O Connections

Pin assignments for the System Input/Output connector are tabulated in Table 3.1.1-1 located at the end of this section. Figure 3.1.1-1 shows the physical arrangement of the connector, which is a 68-Pin 2-Row 0.050-inch subminiature connector that is designed to mate with Robinson-Nugent Model P50E-068-S-TG or equivalent cable socket connector. Unused pins can be left disconnected in most applications, but grounding of the GROUND SENSE input line to ANA RTN can minimize the injection of noise into the card when operating in high-noise environments.

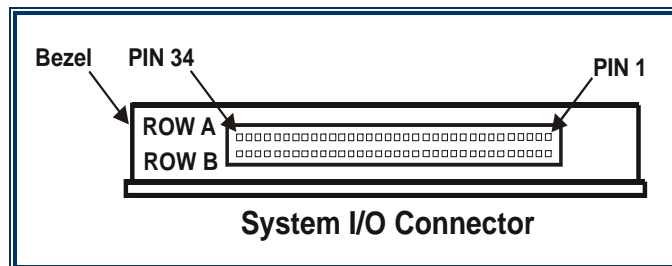


Figure 3.1.1-1. System I/O Connector

3.1.2 System Cabling

If discrete-wire system cabling is used, analog output lines should be arranged into twisted pairs, with the OUT and RTN lines for each channel twisted together. If ribbon cable is used, the wire sequence is ordered in a manner that positions each OUT/RTN output pair as adjacent wires within the cable.

3.2 Analog Outputs

All 16 analog output channels are single-ended, and are intended to drive floating loads, or loads that are common to a ground point that is within ± 1 -Volt of the PCI bus ground.

For loads that are not floating but that have a common ground point, connecting the GROUND SENSE input to the common ground can reduce errors due to a potential on the remote ground. Remote sensing must be enabled through the application software in order to implement this connection.

Consideration should be given to the voltage drop in the output and return lines when operating into significant loads. For example, a 1-milliamp load will produce a line drop of approximately 60 μ V per foot in #28 AWG copper wire. In a long cable, this drop could be significant when using a ± 2.5 V output range, for which 1-LSB is equivalent to 76 μ V.

3.3 External Clock and Trigger

External clocking and burst triggering can be implemented through the control software. If either or both of these features are to be implemented, the card must be wired accordingly.

3.3.1 Clock and Trigger Inputs

To connect the card for external clocking, connect the external clock source to the CLOCK INPUT pin, and the clock source return to DIG RTN. Similarly, for external burst triggering, connect the trigger source to the TRIG INPUT pin. The CLOCK and TRIG inputs accept standard TTL levels, and provide an internal 4.7K pullup resistance to +5 Volts. Both inputs are active on the falling (LOW) edges of the input signals.

3.3.2 Multicard Clocking and Burst Triggering

For multicard synchronous analog input sampling, one of the cards is designated as the **initiator**, and the remaining cards are designated as **targets**. If external clock and trigger sources are to be used, the clock and trigger inputs for the initiator are connected as described in Paragraph 3.3.1. If external signals are not required, the clock and trigger input connections at the initiator can be left disconnected.

The CLOCK OUTPUT signal from the initiator is connected to the CLOCK INPUT pin of one of the target cards, designated as Target-1. If more than one target card is present, the CLOCK OUTPUT from Target-1 is connected to the CLOCK INPUT pin of TARGET-2, and this sequence is repeated for all remaining target cards. The CLOCK OUTPUT from the last target in the chain is not connected.

For multicard synchronous scan triggering, the TRIG OUTPUT and TRIG INPUT connections between cards are configured as described above for synchronous output clocking.

3.4 Digital Input/Output

Digital lines DIG IO 00 through DIG IO 07 are bidirectional, with the signal direction controlled by the control software. DIG AUX 00 is a digital input-only pin, and DIG AUX 01 is a digital output-only pin. DIG AUX 00 and DIG IO 00 through DIG IO 07 are provided with internal 4.7K pullup resistors to +5 Volts. All ten digital lines are compatible with standard TTL levels.

3.5 Physical Installation

Before removing the PMC module from the protective antistatic shipping envelope, ensure that the host board on which the module is to be installed is ready to receive the module. The host panel opening and the mating mezzanine connectors should be free of obstructions such as protective covers and filler panels. After removing the PMC module from the antistatic shipping envelope, remove and save any mounting screws that may be installed in the bezel and standoffs.

Position the PMC module above the host as shown in Figure 3.5-1, with the PCI mezzanine connectors facing the host board, and with the I/O connector and bezel oriented toward the front panel of the host. Carefully insert the bezel of the module through the appropriate opening in the host panel, and align the PCI mezzanine connectors at the rear of the module with the mating connectors on the host. Press the rear of the module carefully but firmly downward onto the host until the bezel and the standoffs are seated against the host board. Verify that the PCI connectors have mated correctly.

Install the four 2.5mm mounting screws supplied with the module, through the host board and into the bezel and the two standoffs on the module. This completes the physical installation of the PMC module.

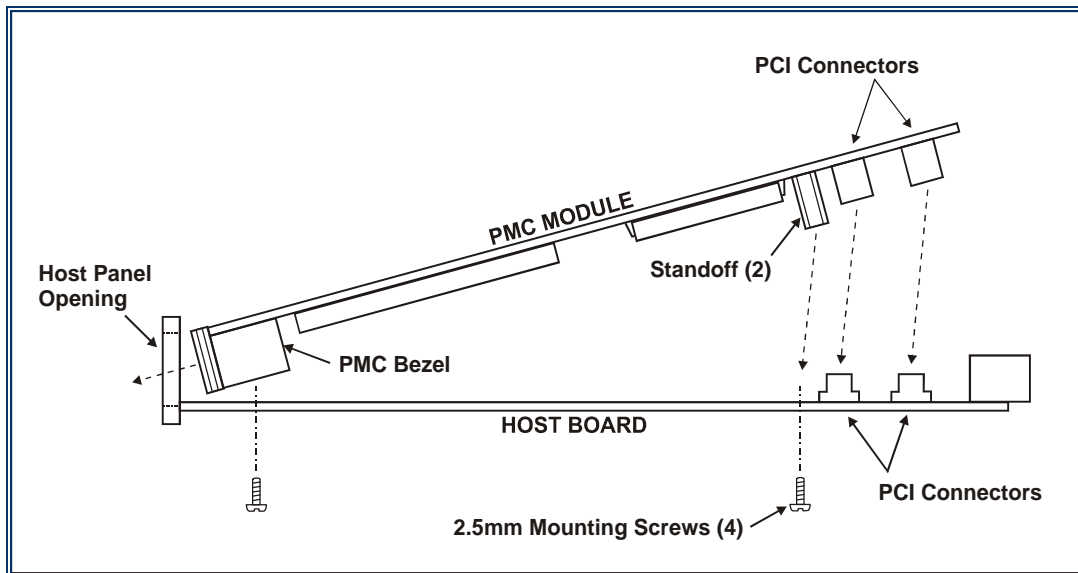


Figure 3.5-1. Physical Installation

3.6 Maintenance

Aside from the usual care associated with precision electronic equipment, this product requires no scheduled maintenance operations. In environments that contain high levels of dust, smoke or other airborne particulate materials, the module should be cleaned periodically to prevent the accumulation of surface deposits that can reduce the ability of power components to dissipate heat.

3.7 Internal Reference Test Point

The internal calibration reference that is used to calibrate all analog output channels during autocalibration is available between the TEST OUT(+) and TEST OUT(-) pins of the I/O connector. Under normal conditions, this reference should not require adjustment. However, if module accuracy appears to degrade, verify that the voltage between these pins conforms to Table 3.7-1. If adjustment is required, adjust the reference trimmer located on the edge of the board until the measured TEST OUT voltage conforms to Table 3.7-1.

Table 3.1.1-1. System I/O Connector Pin Functions

PIN	FUNCTION	PIN	FUNCTION
1A	DIG RTN	1B	DIG RTN
2A	TRIG INPUT	2B	TRIG OUTPUT
3A	DIG RTN	3B	DIG RTN
4A	CLOCK INPUT	4B	CLOCK OUTPUT
5A	ANA RTN	5B	DIG RTN
6A	GROUND SENSE	6B	DIG IO 00
7A	OUTPUT RTN 00	7B	DIG RTN
8A	ANA OUT 00	8B	DIG IO 01
9A	OUTPUT RTN 01	9B	DIG RTN
10A	ANA OUT 01	10B	DIG IO 02
11A	OUTPUT RTN 02	11B	DIG RTN
12A	ANA OUT 02	12B	DIG IO 03
13A	OUTPUT RTN 03	13B	DIG RTN
14A	ANA OUT 03	14B	DIG IO 04
15A	OUTPUT RTN 04	15B	DIG RTN
16A	ANA OUT 04	16B	DIG IO 05
17A	OUTPUT RTN 05	17B	DIG RTN
18A	ANA OUT 05	18B	DIG IO 06
19A	OUTPUT RTN 06	19B	DIG RTN
20A	ANA OUT 06	20B	DIG IO 07
21A	OUTPUT RTN 07	21B	DIG RTN
22A	ANA OUT 07	22B	DIG RTN
23A	OUTPUT RTN 08	23B	DIG RTN
24A	ANA OUT 08	24B	DIG AUX 00 (Input)
25A	OUTPUT RTN 09	25B	DIG RTN
26A	ANA OUT 09	26B	DIG AUX 01 (Output)
27A	OUTPUT RTN 10	27B	DIG RTN
28A	ANA OUT 10	28B	ANA RTN
29A	OUTPUT RTN 11	29B	OUTPUT RTN 13
30A	ANA OUT 11	30B	ANA OUT 13
31A	OUTPUT RTN 12	31B	OUTPUT RTN 14
32A	ANA OUT 12	32B	ANA OUT 14
33A	TEST OUT(-)	33B	OUTPUT RTN 15
34A	TEST OUT(+)	34B	ANA OUT 15

Table 3.7-1. Internal Reference Voltage

FULLSCALE RANGE	INTERNAL REFERENCE VOLTAGE
±2.5V	+2.4999V ±0.0004V
±5V	+4.9997V ±0.0006V
±10V	+9.9994V ±0.0008V

SECTION 4.0 FUNCTIONAL DESCRIPTION

This section provides an overview of the interfaces, internal functions and operating principles that constitute the PMC-3311 module.

4.1 External Interfaces

Two electrical interfaces provide connections between the PMC-3311 module and external system components. The host board controls the module through two PCI bus connectors that mate with two corresponding connectors located on the host (Figure 4.1-1). These connectors provide a standard 32-bit, 33 MHz PCI control interface that conforms to the IEEE PCI local bus specification Revision 2.2. The PCI interface also supplies +5 VDC power for the module, and exchanges output data and control/status information with the host.

A system input/output connector supplies the second electrical interface, which provides connections to system signals that are external to both the host and the host assembly. The I/O connector is located in an access opening in the front panel of the host board, and is designed to interface electrically and mechanically with conventional system cabling. All analog outputs, digital I/O signals and external clock and trigger signals pass through the system I/O connector.

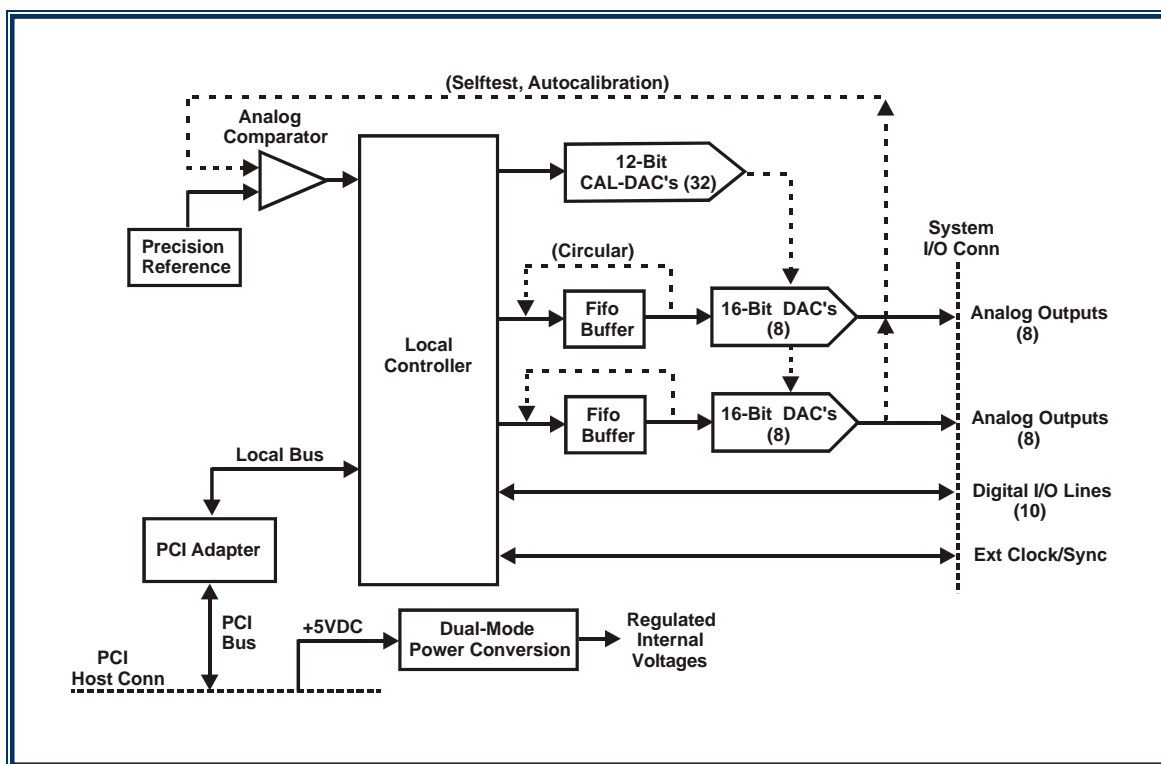


Figure 4.1-1. Functional Diagram

4.2 Control

A PCI interface adapter converts the control functions at the PCI interface into a local bus that is controlled in turn by a local controller. In addition to responding to host commands from the PCI interface adapter, the local controller performs all internal control operations for the module, including output clocking, data buffer access, digital I/O and autocalibration.

4.3 Electrical Power Conversion

Electrical power is obtained through the PCI interface as +5 VDC. To produce the various regulated power voltages that are required by the analog section of the module, the +5 VDC input is first converted by DC/DC switching converters into preregulated voltages that range from approximately +6 VDC to ± 17 VDC. These voltages then are postregulated to the final required output levels by series regulators that ensure high-quality power rails.

4.4 Analog Output Functions

Sixteen analog output channels are driven from two independent FIFO buffers to provide two distinct 8-channel analog output ports. Each buffer can be clocked from a variety of sources, including an internal rate generator or from an external hardware clock. The single-ended outputs can be supplied with a range of ± 2.5 V, ± 5 V or ± 10 V. A remote ground-sensing input provides correction for small potential differences between system grounds.

During autocalibration, each output is driven alternately to zero and fullscale. The output level is compared with a precision internal reference voltage to determine if the output is above or below the reference value. Each output channel contains two 12-bit calibration DAC's for offset and gain corrections.

Autocalibration is executed on-demand by the host, and performs a 12-bit successive-approximation sequence of corrections to both the gain and offset errors of each analog output channel. The final correction values are retained until the module is reset or power is removed. The calibration reference that is used during autocalibration is available for monitoring at a test pin in the system I/O connector.

4.5 External Clock and Trigger

Both the output clocking rates and the trigger rate of function bursts are software controlled through internal dividers that operate from the module's master clock. The outputs from each of these dividers can be replaced with an external digital input, which then controls the associated clock or trigger function.

Digital clock and trigger outputs permit multiple modules to be clocked and triggered simultaneously by connecting the clock and trigger outputs from one module to the clock and trigger inputs of other modules in a daisy-chain sequence. One of the interconnected modules serves as a clock/trigger initiator, and the remaining modules perform as clock/trigger targets.

4.6 Digital Input/Output Port

The digital I/O port consists of eight bidirectional signals, one input-only signal, and one output-only signal. These digital signals are TTL compatible and use the host PCI bus ground as a digital return. All eight bidirectional signals are configured simultaneously as either inputs or outputs by the host, and are supported by a 256-byte FIFO buffer. The buffer is clocked from an internal rate generator, and can be used to generate continuous, one-shot, or periodic bit patterns. The digital port also can be synchronized to analog output clocks or triggers.

APPENDIX A
SUPPLEMENTARY MATERIAL



