



PMC-2215

**High-Speed 8-Channel
16-Bit PMC Analog Input/Output Card**

REFERENCE MANUAL

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**SECTION 1.0
OVERVIEW**

1.1 Product Summary

The PMC-2215 is a single-width PCI mezzanine card (PMC) that provides access to four analog input channels and four analog output channels through a standard 32-Bit, 33MHz PCI bus interface. This product conforms to the mechanical and electrical requirements of the IEEE-1386 standard for common mezzanine cards, and complies with IEEE PCI local bus specification Revision 2.2.

Four 16-Bit analog inputs can be sampled simultaneously at rates to 1.0 MSPS (megasamples per second) per channel, for an aggregate throughput of 4.0 MSPS. The inputs also can be configured in sequenced groups for effective per-channel sample rates up to 2.0MSPS. Analog input data is buffered to the PCI bus through a 64 K-Sample FIFO. Clocking and triggering can be controlled with internal rate generators or from external hardware inputs. Fullscale output ranges can be supplied as ± 2.5 , ± 5 or ± 10 Volts.

Four 16-Bit analog outputs can be clocked simultaneously at rates to 1.0 MSPS, for an aggregate throughput of 4.0 MSPS. Output data is buffered from the PCI bus through a 64 K-Sample FIFO. Clocking and triggering can be controlled with internal rate generators or from external hardware inputs. The internal rate generator can be controlled dynamically from within output functions. Fullscale output ranges can be selected as ± 2.5 , ± 5 or ± 10 Volts, and remote ground sensing ensures maximum accuracy at the loads.

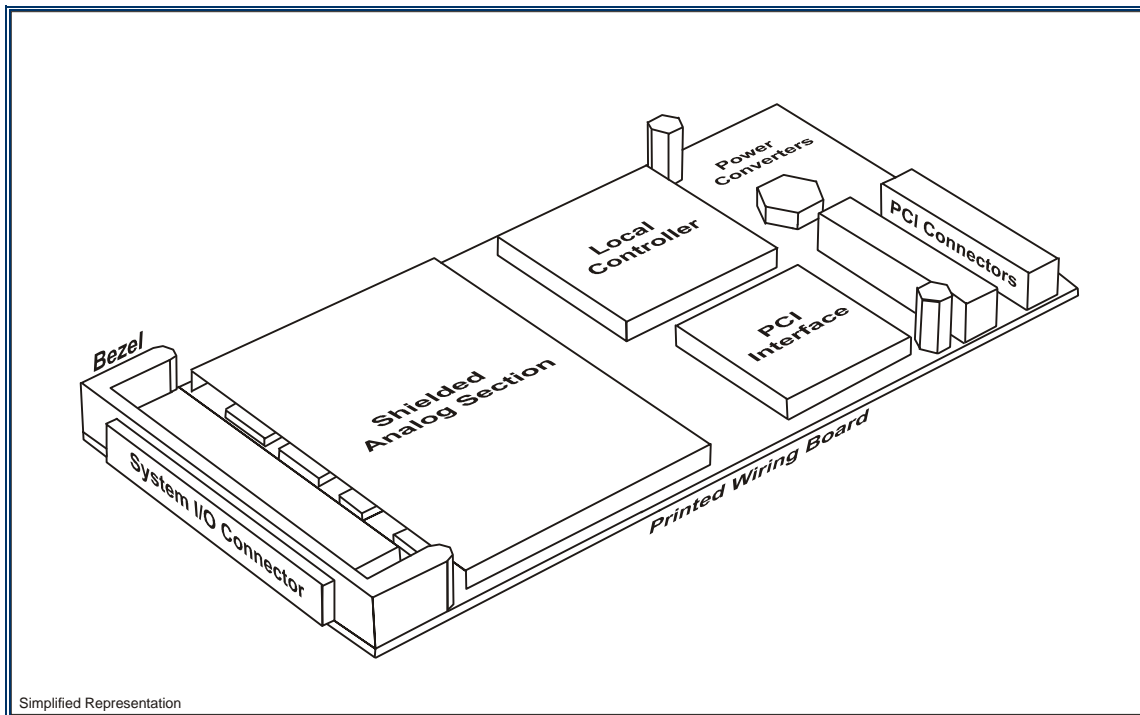


Figure 1.1-1. Physical Organization

A byte-wide bidirectional digital I/O port uses a 1024-Byte FIFO buffer to support pattern generation and capture, or the port can be used for routine digital I/O functions.

Input connections from the system are accepted at the front panel through a standard 68-pin 0.05" subminiature-D male connector. Power requirements consist of a single +5 Volt source obtained from the PMC host. Figure 1.1-1 shows the general locations of major functions and components.

1.2 Mechanical Outline

This product conforms to the mechanical constraints shown in Figure 1.2-1, in compliance with the IEEE-1386 standard for common mezzanine cards.

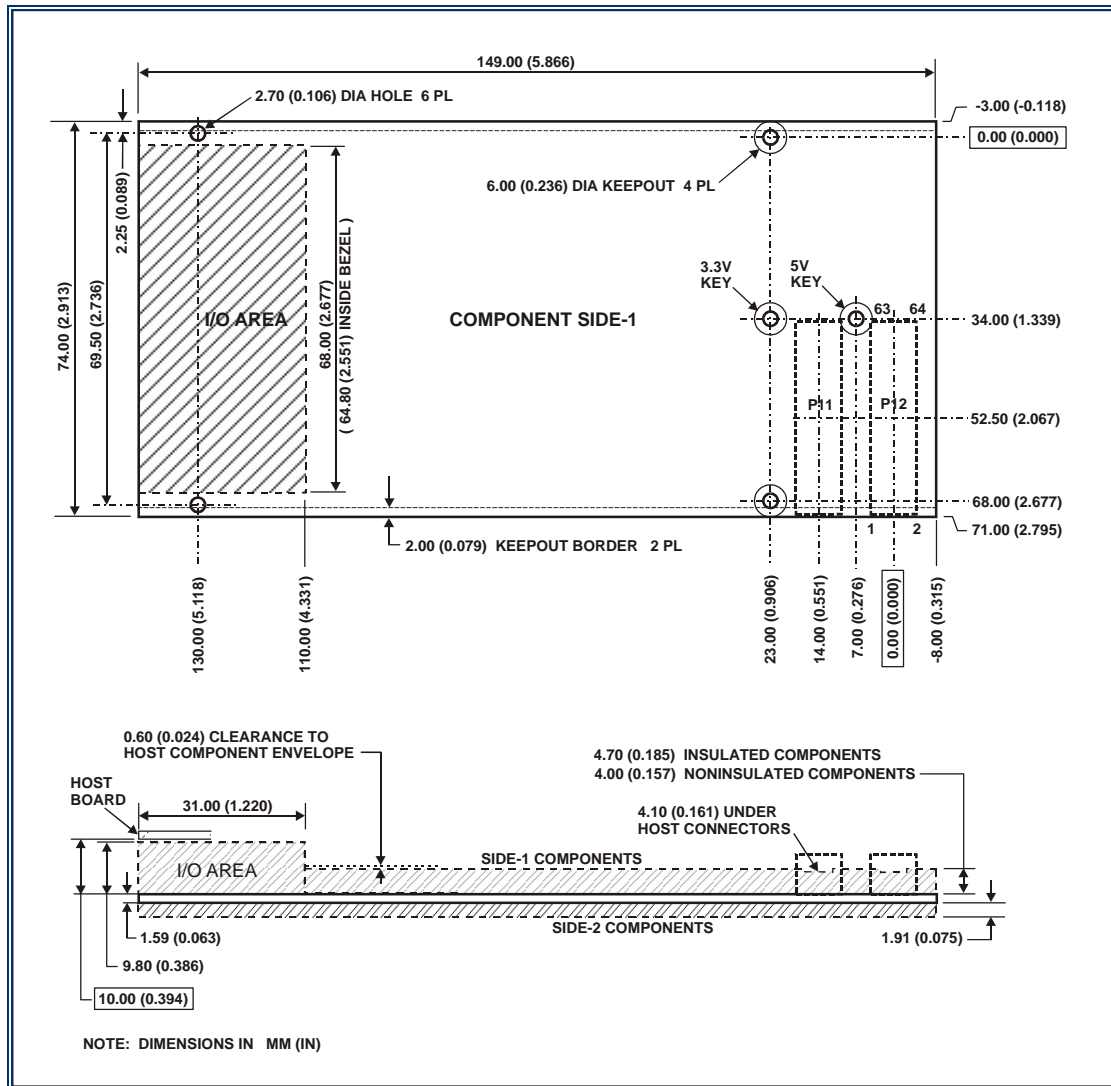


Figure 1.2-1. PMC Mechanical Detail

1.3 Document Scope

This reference manual describes the control characteristics and hardware installation requirements for the PMC-2215 card, and provides a functional description of internal hardware operation. Although occasional references are made to performance characteristics, the product specification SPEC-PMC2215 is the controlling document for performance parameters. An electrical schematic, if provided with this manual, represents the hardware configuration at the time of issue.

SECTION 2.0

CONTROL

2.1 Introduction

The control interface for the PMC-2215 complies with the IEEE PCI local bus specification Revision 2.2 for a 32-bit data bus and a 33 MHz PCI clock. A PCI-9054 PLX™ PCI adapter provides communication between the PCI bus and the local control bus. The module occupies 128 contiguous bytes of control space, and can be located on any 32-longword boundary in memory.

Local control registers, shown in Table 2.1-1, are accessed with single read or write operations, while three FIFO buffer access registers support both single transactions and mastered DMA transactions. A single interrupt on the PCI INT-A line can respond to any of multiple selectable events. To ensure compatibility with subsequent firmware extensions, only zero-states should be written to control fields that are identified as "reserved."

The board control register (BCR) shown in Table 2.1-2 provides individual clearing functions for the three internal buffers, and gating functions for five rate generators. The BCR also controls the data coding format and provides a control bit for initializing the board. A single control bit initializes autocalibration.

2.2 Reset and Initialization

A reset command from the PCI bus initializes both the PCI adapter and the local controller. The local controller autoloads configuration information from internal EPROM, and then initializes all internal registers to default values. The total time required for these operations is 300 milliseconds or less. The PCI interrupt is disabled after a PCI reset occurs.

The local controller can be initialized without reconfiguring either the PCI adapter or the controller by setting the INITIALIZE control bit HIGH in the BCR. Local controller initialization requires 30 milliseconds or less for execution, after which the control bit is cleared automatically and the local interrupt is asserted.

Upon completion of reset or initialization, the board is in the following state:

- ◆ Control registers are in their default states
- ◆ Data buffers are cleared (empty)
- ◆ Analog inputs are configured for simultaneous-quad software clocking
- ◆ Analog outputs are configured for simultaneous software clocking
- ◆ Analog Inputs and outputs are configured for continuous triggering
- ◆ Input/Output range is ± 10 Volts
- ◆ Analog outputs are initialized to midrange (zero)
- ◆ Analog input/output and digital I/O clocking is disabled
- ◆ Analog I/O clock rate generators are adjusted to 720 kHz, and are disabled
- ◆ Analog I/O trigger rate generators are adjusted to 100 kHz, and are disabled
- ◆ Digital bidirectional I/O lines are configured as Direct-I/O inputs
- ◆ The digital I/O port clock rate generator is adjusted to 18 MHz, and is disabled.

2.3 Analog Inputs

2.3.1 Functional Organization

Four analog input channels are arranged into two channel groups, as shown in Figure 2.3.1-1. Both groups can be sampled simultaneously, or each group can be sampled on alternate input clocks to effectively double the input sampling rate for two channels (See Section 2.3.7). The two groups are designated as odd and even, with Channels 01 and 03 assigned to the odd group and Channels 00 and 02 to the even group. This arrangement preserves the separate clocking capability for boards that have only two channels (00, 01) installed.

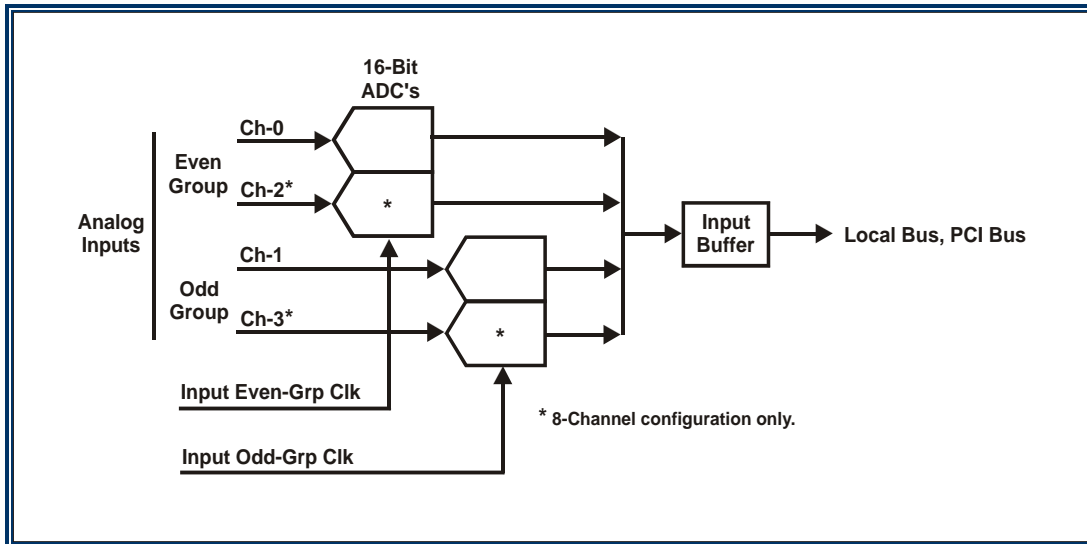


Figure 2.3.1-1. Analog Inputs

All analog input data flows through a single FIFO buffer to the local bus, and from the local bus to the PCI bus. The analog inputs can be clocked independently of the analog outputs, or both can be clocked synchronously. Control of the analog input buffer is described in Section 2.3.4, which also identifies the available data coding formats.

2.3.2 Channel Selection

2.3.2.1 Enabling Mask

Each analog input or output channel is designated as either active or inactive through the Channel-Enable Mask register shown in Table 2.3.2.1-1. A channel is designated as **active** by setting the corresponding mask bit HIGH, or as **inactive** by clearing the bit LOW. During initialization, all channels are designated as active.

Note: The default mask value of 0x0000 0F0F applies to all board configurations. For boards that have only four resident channels, mask bits corresponding to nonexistent channels have no effect and can be either cleared or left asserted after initialization.

2.3.2.2 Channel Scan

An input **scan** is an analog input channel group that contains all active input channels. A scan commences with the lowest-numbered channel, and proceeds upward consecutively through all active channels. The term **scan**, as it is used here, does not imply a sequential operation at the hardware level, but indicates the ordering of data in the input buffer.

2.3.3 Analog Input Control Register

The Analog Input Control register (Table 2.3.3-1) controls analog input clocking, burst triggering, and buffer clearing. The register also contains the input buffer threshold flag and provides a control bit for selecting *sequenced* sampling.

Note: For sampling rates above 800kHz, the WARP MODE control bit in the analog input control register must be asserted HIGH (See note in Section 2.3.5.1).

2.3.4 Analog Input Buffer

The analog input data buffer has a capacity of 64K-Samples (optionally 16K), and can be accessed either by single PCI-read transactions, or through mastered DMA transactions. Access to this buffer is provided through the Input Buffer register shown in Table 2.3.4-1. The buffer register contains an 18-Bit active field, with the lower 16 bits dedicated to input data, and the upper two bits used as status flags. PCI bus data written to the analog input buffer is ignored.

The analog input buffer can be cleared to empty by asserting either the CLEAR ANALOG INPUT BUFFER control bit HIGH in the BCR, or the duplicate control bit in the analog input control register. All clear-buffer control bits clear automatically after assertion.

2.3.4.1 Data Field and Coding Format

The 16-Bit data fields in both the analog input and analog output data buffers contain right-justified data in either offset binary or two's complement format (Figure 2.3.4.1-1). If the OFFSET BINARY DATA control bit is HIGH (default) in the BCR, analog input and output data are coded in offset binary format. If the control bit is LOW, data is coded in two's complement format.

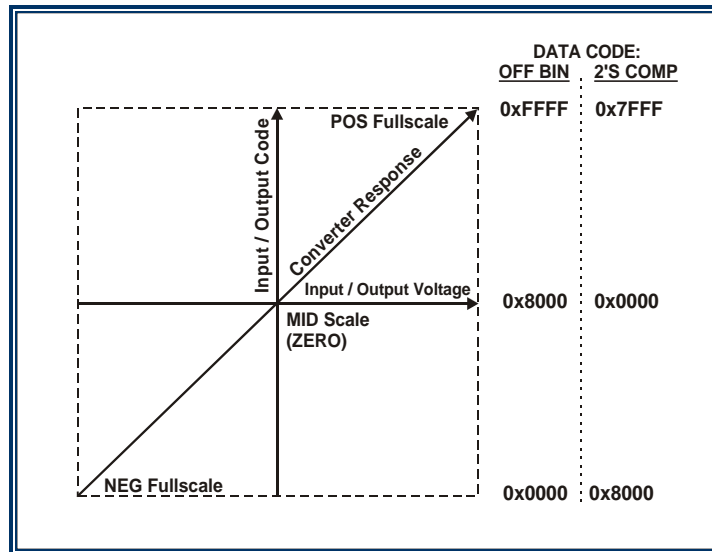


Figure 2.3.4.1-1. Analog Data Coding Formats

2.3.4.2 Threshold Registers

2.3.4.2.1 Thresholds

Two threshold registers for the analog input buffer provide a flag for controlling data flow to and from the buffer. HIGH and LOW thresholds are specified through the high and low threshold registers shown in Table 2.3.4.2-1. Each threshold represents a specific number of output values in the buffer, and can have any integer value from zero up to the capacity of the buffer.

The high and low thresholds define a range within which the BUFFER THRESHOLD FLAG bit in the analog input control register is HIGH. The BUFFER THRESHOLD FLAG is HIGH if the number of values (samples) in the buffer is greater than the **low** threshold **and also** is less than or equal to the **high** threshold. The flag is LOW if the number of samples in the buffer is outside of the specified range. The buffer threshold flag is duplicated in the BCR.

An interrupt (Section 2.6) can be specified to occur on a HIGH-to-LOW transition of the threshold flag. This transition indicates that the number of samples in a buffer has moved outside of the specified range.

The data and status fields of the analog input buffer register are shown in Table 2.3.4-1. Analog input data occupies the lower 16 bits of the 18-bit active field. The two upper bits are status flags that indicate the last value in a triggered burst, and the even/odd status of the associated data channel.

2.3.4.2.2 Data Streaming

The threshold range provides a convenient means of controlling the continuous flow of data from the board to the PCI bus. For example, using the default values of 0xD000 and 0x3000 for the high and low thresholds, the threshold flag will undergo a HIGH-to-LOW transition each time the number of samples in the buffer moves above 0xD000 or below 0x3000, and the following sequence will stream data from the board:

1. Select the "Input Buffer threshold flag HIGH-to-LOW transition" in Table 2.6-1.
2. Enable input clocking.
 3. Wait for the interrupt (number of samples exceeds 0xD000).
 4. Clear the interrupt response status bit in Table 2.6-1.
 5. Transfer a block of data $\leq 0xD000$ from the input buffer.
6. Repeat Steps 3-5 to sustain the data stream.

2.3.5 Input Clocking

2.3.5.1 Clock Source Selection

Clocking for the analog inputs can be selected from any of the various sources shown in Figure 2.3.5.1-1 with the INPUT CLOCK SOURCE control field in the Analog Input Control register (Table 2.3.3-1). For sampling rates above 800kHz, the WARP MODE control bit in the input control register must be asserted HIGH.

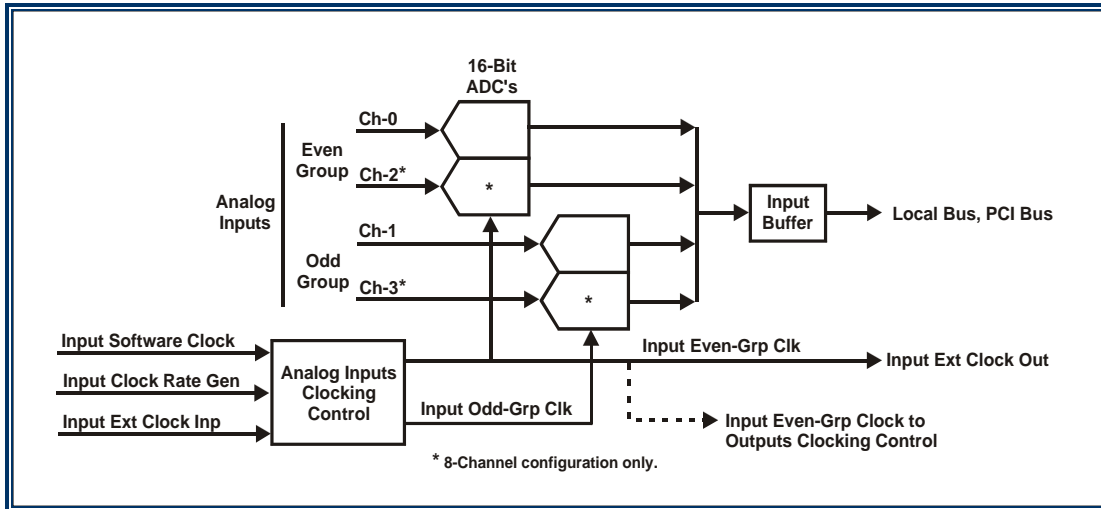


Figure 2.3.5.1-1. Analog Input Clocking

Note: At input sampling rates above 800KSPS, all ADC's must be placed in the "WARP" mode by setting the WARP MODE control bit HIGH in the analog input control register. In this mode, the maximum delay between samples is 1.0 millisecond, after which the next sample is considered to be invalid. For this reason, the first sample taken after a 1.0 millisecond delay between samples is automatically discarded, and a second sample is taken immediately.

This issue affects only the first sample taken after clocking is enabled, and the first sample in a burst if the separation between bursts exceeds 1.0 millisecond.

An **input software clock** is generated by asserting the INPUT SOFTWARE CLOCK control bit HIGH in the control register, when the READY FOR INPUT CLOCK status bit is HIGH. The control bit clears automatically. The READY FOR INPUT CLOCK status bit is LOW during ADC conversions, and is HIGH when the ADC's are ready to accept a new clock.

The **input clock rate generator** provides an output clocking frequency that is divided from the local master clock frequency of 36 MHz.

An **input external clock** occurs at each HIGH-to-LOW transition of the external hardware clock input line at the system I/O connector, and permits clocking of the analog outputs from an external clock source. The **input external clock output** line in the system I/O connector is asserted LOW each time an input even-group clock occurs, and can be used to synchronize analog input clocking on multiple boards.

The digital I/O port also can be clocked from the analog input clock.

2.3.5.2 Enabling Input Clocking

Clocking of the analog inputs is enabled and disabled with the ENABLE INPUT CLOCKING control bit in the BCR.

Note: Regardless of which clock source is selected, actual clocking of the inputs will not commence until the ENABLE INPUT CLOCKING control bit is set HIGH. The ENABLE INPUT CLOCKING control bit should be LOW while analog input control parameters are being configured.

2.3.5.3 Input Clock Rate Generator

The Input Clock Rate Generator is enabled and disabled by the ENABLE INPUT CLOCK RATE GEN control bit in the BCR. The rate generator is enabled when this control bit is HIGH, and is disabled when the bit is LOW.

The frequency of the analog input clock rate generator is controlled up to 2.0MHz by the 16-bit RATE DIVISOR control field in the Input Clock Rate Generator control register (Table 2.3.5.3-1). With a value of **Nclk** in the register, the clocking frequency **Fclk** is:

$$Fclk = 36,000 / Nclk,$$

where **Fclk** is in kilohertz, and **Nclk** can be any integer from 18 to 65535. The clocking rate for the analog inputs in samples-per-second equals the generator frequency in Hertz.

Note: The maximum analog input clocking rate is 1.0MHz in the *simultaneous* sampling mode, and 2.0 MHz in the *sequenced* sampling mode (Section 2.3.7).

For sampling rates above 800kHz, the WARP MODE control bit in the analog input control register must be asserted HIGH (See note in Section 2.3.5.1).

2.3.6 Input Triggering Modes

2.3.6.1 Continuous Sampling

In the *continuous* triggering mode, analog input clocking from the selected clock source proceeds continuously as long as clocking is enabled and the input buffer is not full. The continuous input sampling mode is selected when the INPUT TRIGGER SOURCE field in the analog input control register is zero.

2.3.6.2 Triggered Bursts

The *triggered burst* mode permits the acquisition of analog input samples in blocks, or bursts, of a specific size. An input burst is initiated by an input trigger, and sampling continues until the number of samples acquired equals the value contained in the Input Burst Size register listed in Table 2.1-1. Sampling then ceases until another trigger occurs. The default value for the input burst size register is 256 samples (0x100).

The size of a burst can be as large as the capacity of the buffer, or as small as a single scan, but must be an integer multiple of the input scan size (number of active input channels). Consecutive sample bursts will accumulate in the input buffer until the buffer becomes full.

Note: The ENABLE INPUT TRIGGERING control bit in the BCR must be HIGH in order to enable analog input triggering. This control bit also enables or disables the input trigger rate generator.

ENABLE INPUT TRIGGERING is ignored if continuous triggering is selected.

2.3.6.3 Trigger Sources

Figure 2.3.6.3-1 illustrates the triggering sources that are available for analog input bursts. An input burst can be triggered from the input trigger rate generator, by a software input trigger, or by an external input hardware trigger. The analog outputs can be configured to trigger synchronously with the analog inputs (Section 2.4.5.5).

The **input software trigger** is generated by asserting the INPUT SOFTWARE TRIGGER control bit HIGH in the analog output control register when the READY FOR INPUT TRIGGER flag is HIGH. The control bit then clears automatically. The READY FOR INPUT TRIGGER flag is LOW during an input burst, and is HIGH between bursts. Triggering is disabled if continuous operation is selected.

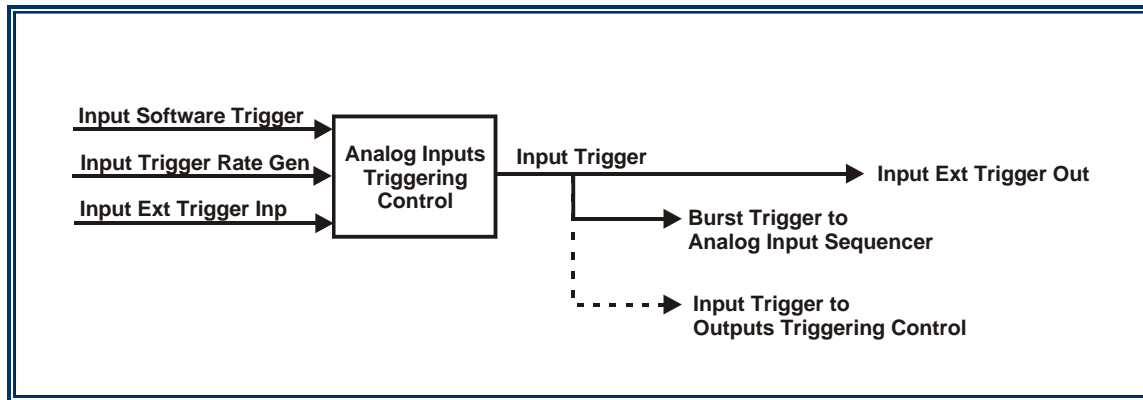


Figure 2.3.6.3-1. Input Burst Triggering

When the **external analog input hardware trigger** is selected, an input trigger occurs on each HIGH-to-LOW transition of the external hardware line *Input Ext Trigger Inp* at the system I/O connector. A LOW pulse is generated at the external hardware output line *Input Ext Trigger Out* each time an input trigger occurs, and can be used to synchronize analog input triggering on multiple boards.

2.3.6.4 Input Trigger Rate Generator

The frequency of the input trigger rate generator is controlled by the RATE DIVISOR value in the Input Trigger Rate Generator control register (Table 2.3.6.4-1). With a value **Ntrig** in the register, the triggering frequency **Ftrig** is:

$$Ftrig = 36,000 \div Ntrig,$$

where **Ftrig** is in kilohertz, and **Ntrig** can be any integer from 36 to 1048575.

2.3.7 Input Sampling Modes

2.3.7.1 Simultaneous Sampling

As Figure 2.3.1-1 indicates, even/odd analog input channels can be clocked separately. The analog inputs can be clocked simultaneously or in even/odd groups, depending on the state of the SEQUENCED SAMPLING control bit in the analog input control register. If SEQUENCED SAMPLING is in the default LOW state, **simultaneous** sampling is selected, and all active inputs are clocked simultaneously.

The maximum input sample rate in the simultaneous sampling mode is 1.0 MHz (See note in Section 2.3.5.1).

2.3.7.2 Sequenced Sampling

If **sequenced sampling** is selected by setting the SEQUENCED SAMPLING control bit HIGH, the even and odd-numbered input active channels are sampled on alternate clocks, and consequently all inputs are sampled at one-half the selected clocking rate. By connecting even/odd input pairs together, the effective clocking rate is doubled to the selected clocking rate, even though the ADC's are being clocked at one-half that rate. In other words, each even/odd sample pair in the input buffer can be considered as two consecutive input samples from a single input.

For example, if the input lines for channels 00 and 01 are connected together, and inputs 02 and 03 are disabled, the first sample in the buffer would be from input 00, the second from 01, the third from 00, etc., producing an input buffer sequence of 00-01-00-01...-00-01. Because inputs 00 and 01 are connected together, each sample in the buffer represents the same input signal.

If inputs 02 and 03 are connected together and if all four input channels are enabled, the buffer sequence becomes 00-01-02-03-01-02...-02-03, where all 00,01 pairs represent one input, and the 02,03 pairs represent the other input.

Because the ADC's are clocked at one-half the selected clocking rate, the maximum clocking rate for sequenced sampling can be increased to 2.0 MHz without exceeding the maximum rate of 1.0 MHz for the ADC's. The number of available input channels is reduced by one half in the sequenced sampling mode, but the available input sampling rate is effectively doubled. Another related issue is input noise, which increases because of the unavoidable mismatch between the ADC's in the even/odd channels.

2.3.8 Multicard Input Synchronization

If the external ADC clock inputs and outputs are interconnected between multiple cards as described in Section 3.4.2, the analog inputs on all of the cards can be clocked synchronously. The first card in the daisy chain is designated as the *initiator card*, and provides the clock signal for all of the other cards in the chain, designated as *target cards*. All target cards have External Analog Input Hardware Clock selected in the INPUT CLOCK SOURCE field of their analog input control registers, and the initiator can be configured for any available clock source. When configured in this manner, the analog inputs of all target cards will clock synchronously with the analog inputs on the initiator.

Similarly, by daisy-chaining the ADC trigger inputs and outputs between the cards, the analog inputs of all target cards can be burst-synchronized to the initiator card. The target cards will have External Analog Input Hardware Trigger selected in the INPUT TRIGGER SOURCE fields of their analog input control registers, and the initiator card can be triggered from any available trigger source. All cards then will initiate an input burst each time an input trigger occurs in the initiator card.

2.3.9 Summary

The following table consolidates the operations involved in establishing an analog input sequence, and lists the default values for all input parameters.

OPERATION	PARAMETER	DEFAULT	SECTION
Disable input clocking and triggering	Clock and trigger enabling control bits in the BCR.	Disabled	2.3.5.2 2.3.6
Establish input parameters	Channel selection	All	2.3.2.1
	Buffer high and low thresholds	HIGH: 0xD000 LOW: 0x3000	2.3.4.2
	Clocking rate	720 KSPS	2.3.5.3
	Triggering mode	Continuous	2.3.6
	Sampling mode	Simultaneous	2.3.7
Enable input clocking and triggering *	Clock and trigger enabling control bits in the BCR.	Disabled	2.3.5.2 2.3.6

* Triggering is automatically enabled in the continuous triggering mode.

2.3.10 Range Control

The input and output voltage range is selected with the INPUT/OUTPUT RANGE control field in the BCR.

2.4 Analog Outputs

2.4.1 Functional Organization

The four analog output channels are driven from a single FIFO buffer that can be operated in either an open mode in which data flows directly through the buffer to the output DAC's, or in a looping mode in which data recirculates within the buffer (Figure 2.4.1-1). The outputs can be clocked either simultaneously or sequentially.

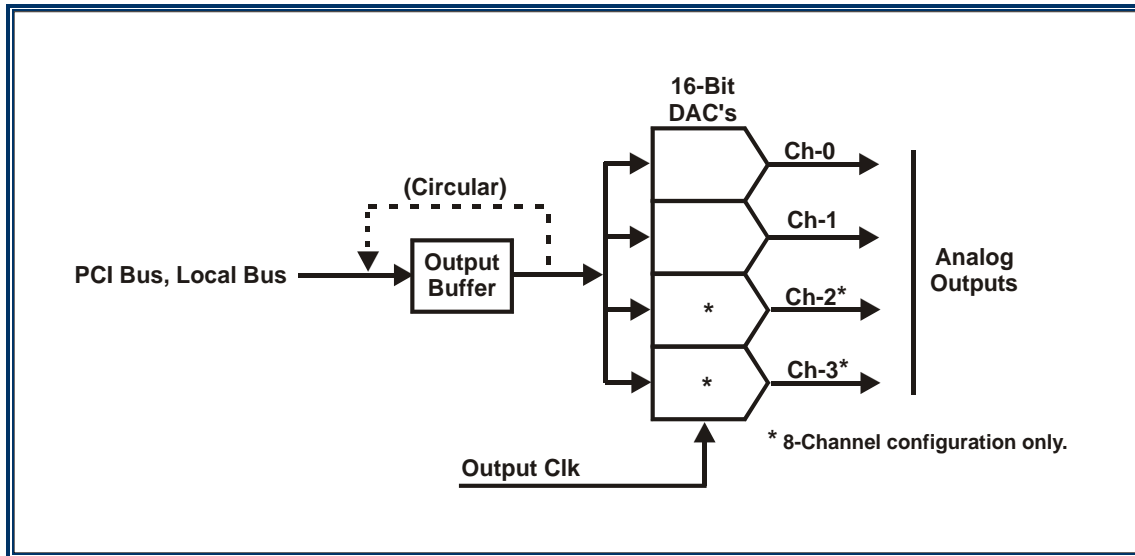


Figure 2.4.1-1. Analog Outputs

When clocking from the Output Clock Rate Generator, the clocking rate can be changed dynamically at specific points in an output function. Both continuous and burst sampling modes are available.

The open buffer configuration is used most commonly in data streaming applications, in which data is clocked continuously from the buffer and is refreshed periodically from the PCI bus. A closed, or looping, buffer recirculates previously loaded data continuously, thereby producing periodic functions. Both the open and closed configurations can be used to generate arbitrary waveforms. Control of the analog output buffer is described in Section 2.4.4, which also identifies the available data coding formats.

2.4.2 Channel Selection

2.4.2.1 Enabling Mask

Each analog output channel is designated as either active or inactive through the Channel-Enable Mask register shown in Table 2.3.2.1-1. A channel is designated as **active** by setting the corresponding mask bit HIGH, or as **inactive** by clearing the bit LOW.

Note: The default mask value of 0x0000 0F0F applies to all board configurations. For boards that have only four resident channels, mask bits corresponding to nonexistent channels have no effect and can be either cleared or left asserted after initialization.

2.4.2.2 Channel Scan

An output **scan** is an analog output channel group that contains all active output channels. A scan commences with the lowest-numbered channel, and proceeds upward consecutively through all active channels. The term **scan**, as it is used here, does not imply a sequential operation at the hardware level, but indicates the ordering of data in the output buffer.

Only active output channels are controlled through the output buffer. Each inactive channel retains either the initial midrange value or, if temporarily active after initialization, the last value received from the buffer.

During initialization, all output channels are designated as active, and the outputs are initialized to midrange (zero).

2.4.3 Analog Output Control Register

Operation of the analog outputs is controlled through a dedicated Analog Output Control register (Table 2.4.3-1) that controls clocking, burst triggering, and looping of the output buffer, as well as buffer clearing.

2.4.4 Analog Output Buffer

The analog output data buffer has a capacity of 64K-Samples (optionally 16K), and can be accessed either by single PCI-write transactions, or through mastered DMA transactions. Access to the buffer is provided through the analog Output Buffer register shown in Table 2.4.4-1. Analog output data occupies the lower 16 bits of the 18-bit active field. The upper two bits control data burst operations and dynamic control of the output clock rate generator. A PCI-read transaction from the output buffer produces an all-zero value.

The analog output buffer can be cleared by asserting either the CLEAR ANALOG OUTPUT BUFFER control bit HIGH in the BCR, or the duplicate control bit in the analog output control register. All clear-buffer control bits clear automatically after assertion

2.4.4.1 Data Field and Coding Format

The data fields for both analog inputs and outputs are described in Section 2.3.4.1.

2.4.4.2 Threshold Registers

Two threshold registers for the analog output buffer operate identically to the analog input buffer threshold registers described in Section 2.3.4.2, and are shown in Table 2.4.4.2-1.

2.4.4.3 Physical Configuration

The analog output buffer can be operated in either an open mode or a looping mode. In the open mode, the buffer output is routed only to the output channels. In the looping, or closed, mode, the output of the buffer is connected to the input of the buffer, and data circulates within the buffer as well as being clocked to the analog outputs.

2.4.4.4 Open Buffer

When operating in the open mode, each output sample is flushed from the buffer as it is clocked to the associated analog output channel. The PCI bus has access to an open buffer, thereby permitting continuous streaming of data from the host to the analog outputs. The open mode is selected for a buffer when the OUTPUT LOOPING control bit is LOW (default) in the analog output control register.

2.4.4.5 Looping (Closed) Buffer

Data within a looping buffer is retained indefinitely within the buffer, and external access from the PCI bus is inhibited. PCI bus data written to a looping buffer is discarded. Because data can neither enter nor leave a looping buffer, the number of samples in the buffer is constant after the looping mode has been selected. The looping mode is selected for a buffer by setting the OUTPUT LOOPING control bit HIGH in the analog output control register.

2.4.5 Output Clocking

2.4.5.1 Clock Source Selection

The analog outputs can be clocked from a number of clock sources, as illustrated in Figure 2.4.5.1-1. The OUTPUT CLOCK SOURCE control field in the Analog Output Control register (Table 2.4.3-1) selects the analog output clocking source.

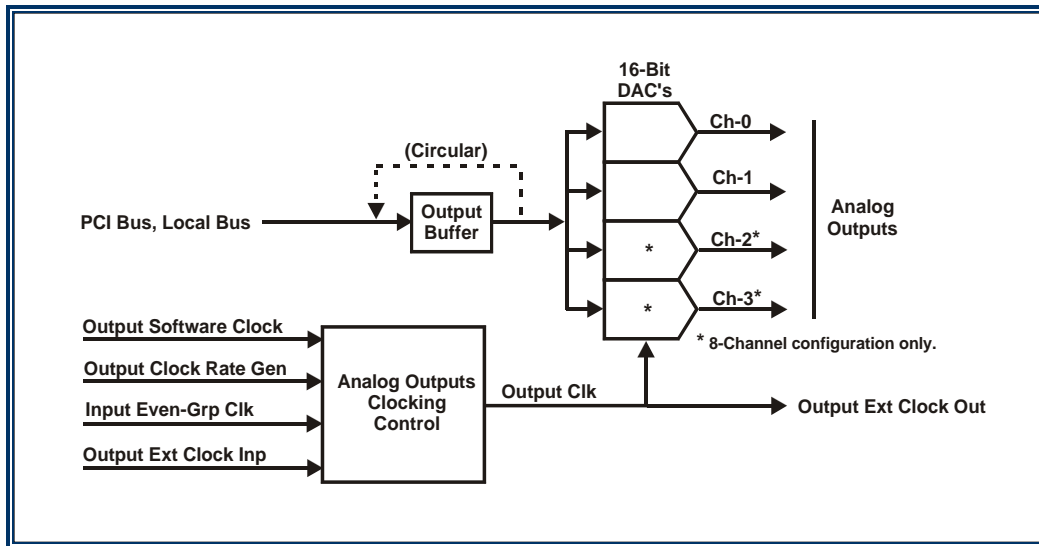


Figure 2.4.5.1-1. Analog Output Clocking

An **output software clock** is generated by asserting the OUTPUT SOFTWARE CLOCK control bit HIGH in the control register, when the READY FOR OUTPUT CLOCK status bit is HIGH. The control bit clears automatically. The READY FOR OUTPUT CLOCK status bit is LOW while data is transferred from the output buffer, and is HIGH when the buffer is ready to accept a new clock.

The **output clock rate generator** provides an output clocking frequency that is divided from the local master clock frequency of 36 MHz.

An **output external clock input** event occurs at each HIGH-to-LOW transition of the external hardware clock input line at the system I/O connector, and permits clocking of the analog outputs from an external clock source. The **output external clock output** line in the system I/O connector is asserted LOW each time an output clock occurs, and can be used to synchronize analog output clocking on multiple boards.

Selection of the **input even-group clock** synchronizes analog output clocking to the analog inputs. To synchronize the digital I/O port with the analog outputs, the digital port also can be clocked from the analog output clock..

2.4.5.2 Enabling Output Clocking

Clocking of the analog outputs is enabled and disabled with the ENABLE OUTPUT CLOCKING control bit in the BCR.

Note: Regardless of which clock source is selected, actual clocking of the outputs will not commence until the ENABLE OUTPUT CLOCKING control bit is set HIGH. The ENABLE OUTPUT CLOCKING control bit should be LOW while analog output control parameters are being configured.

2.4.5.3 Output Clocking Modes

2.4.5.3.1 Simultaneous Clocking

The more common clocking mode is *simultaneous clocking*, in which all samples in a scan appear simultaneously at their corresponding outputs. The sample value for each channel in a scan is extracted from the buffer and stored in an intermediate register until the last sample in the scan is transferred from the buffer. When the last sample appears at the buffer output, all samples in the scan are transferred simultaneously to their respective outputs when the next output clock occurs.

Simultaneous clocking is selected when the SEQUENTIAL OUTPUT CLOCKING control bit is LOW (default) in the analog output control register.

2.4.5.3.2 Sequential Operation

When *sequential clocking* is selected, each sample in the buffer is clocked individually to the corresponding output, without regard to the sample's position in a scan. Scan boundaries have no effect during sequential clocking. For example, a series of five scans, each of which contains three active channels, would require 15 sample clocks to write all values to the outputs.

Sequential clocking is selected by setting the SEQUENTIAL OUTPUT CLOCKING control bit HIGH in the analog output control register.

2.4.5.4 Output Clock Rate Generator

The Output Clock Rate Generator is enabled and disabled by the ENABLE OUTPUT CLOCK RATE GEN control bit in the BCR. The rate generator is enabled when this control bit is HIGH, and is disabled when the bit is LOW.

2.4.5.4.1 Frequency Control

The frequency of the analog output clock rate generator is controlled up to 1.0MHz by the 16-bit RATE DIVISOR control field in the Output Clock Rate Generator control register (Table 2.4.5.4.1-1). With a value of **Nclk** in the register, the clocking frequency **Fclk** is:

$$\mathbf{Fclk} = 36,000 \div \mathbf{Nclk},$$

where **Fclk** is in kilohertz, and **Nclk** can be any integer from 36 to 65535. The clocking rate for the analog outputs in samples-per-second equals the generator frequency in Hertz.

2.4.5.4.2 Dynamic Rate Control

When the analog output buffer is operating from the output clock rate generator, the frequency of the rate generator can be changed dynamically, or 'on the fly', at any point in an output function. The RATE CHANGE control bit in the buffer data register, when HIGH, changes the context of the OUTPUT DATA field from "output data" to "rate-generator divisor."

If dynamic rate control is implemented, the rate-change occurs at the beginning of the scan for which the new rate is to be applied. The sample data values for the scan then follow the rate-change value in the buffer.

A rate-change value consists of the OUTPUT DATA field, and the RATE CHANGE control bit, which is asserted HIGH for the rate-change buffer value. The OUTPUT DATA field in the rate-change value replaces the **Nclk** divisor that is used to calculate the output clock rate generator frequency **Fclk** in Section 2.4.5.4.1. The clocking rate changes to the new frequency when the scan in which it is inserted appears at the analog outputs.

Note: The value contained in the Output Clock Rate Generator register is unaffected by dynamic rate control operations.

The frequency of the rate generator can be changed repeatedly throughout an output function, and the last selected frequency will be retained until clocking is disabled or the board is initialized. When clocking is disabled, control of the rate generator is restored to the output clock rate generator control register.

2.4.5.5 Synchronous Clocking

Output clocking can be synchronized to analog input clocking by selecting the Analog Input Clock with the OUTPUT CLOCK SOURCE field in the analog output control register. In this configuration, the outputs clock simultaneously with the inputs, regardless of the source of analog input clocking.

The digital I/O port (Section 2.5) also can be synchronized to the analog inputs.

2.4.6 Output Sampling Modes

2.4.6.1 Continuous Sampling

In the *continuous sampling* mode, data flows through the output buffer to the analog outputs continuously as long as clocking is enabled and the buffer is not empty. The continuous output sampling mode is selected when the OUTPUT TRIGGER SOURCE field in the analog output control register is zero.

2.4.6.2 Triggered Bursts

The *burst sampling* mode permits the clocking of the analog outputs to be initiated and terminated at specified function boundaries. An example of this configuration is the generation of a complex transient waveform that occurs periodically with a low duty cycle. With continuous sampling, the buffered function would have to encompass the entire period of the transient, even though most of the samples might be zero or some other constant value. By using burst sampling however, only the transient waveform must be stored in the buffer.

A burst is initiated by a burst trigger, and is terminated by an END OF BURST (EOB) flag in the buffer data sequence. The trigger can originate from a number of sources as described in Section 2.4.6.3, and the EOB flag is controlled through the output data buffer.

To identify the last sample in a sequence, the EOB control bit in the buffer data register is set HIGH in the data word that contains the last sample value in the burst. The burst then will terminate after the data sample that accompanies the EOB flag has been transferred to the associated analog output.

The analog output buffer can contain multiple burst functions simultaneously. Multiple bursts are executed sequentially, with each burst initiated by a trigger and terminated by an EOB flag.

NOTE: The ENABLE OUTPUT TRIGGERING control bit in the BCR must be HIGH in order to enable analog output triggering. This control bit also enables or disables the output trigger rate generator.

2.4.6.3 Trigger Sources

Figure 2.4.6.3-1 illustrates the triggering sources that are available for analog output bursts. An output burst can be triggered from the output trigger rate generator, by a software output trigger, or by an external output hardware trigger. Output bursts also can be synchronized to analog input bursts by selecting the input trigger.

The **software trigger** is generated by asserting the OUTPUT SOFTWARE TRIGGER control bit HIGH in the analog output control register when the READY FOR OUTPUT TRIGGER flag is HIGH. The control bit then clears automatically. The READY FOR OUTPUT TRIGGER flag is LOW during an output burst, and is HIGH between bursts. Triggering is disabled if continuous operation is selected.

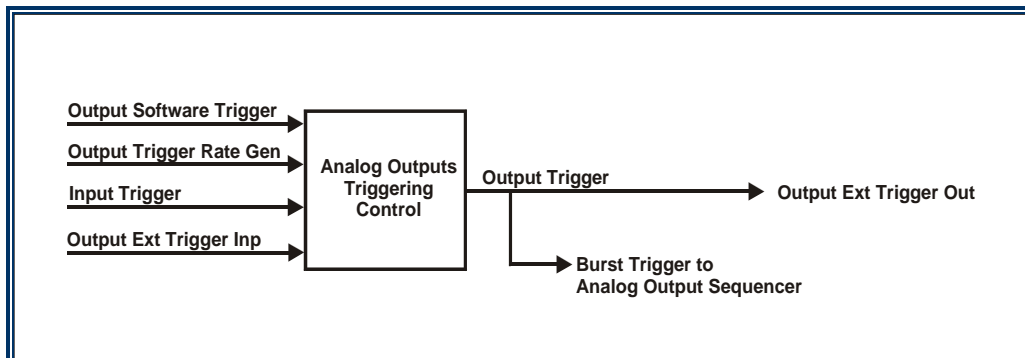


Figure 2.4.6.3-1. Output Burst Triggering

When **external analog output triggering** is selected, an output trigger occurs on each HIGH-to-LOW transition of the external hardware input *Output Ext Trigger Inp* at the system I/O connector. A LOW pulse is generated at the external hardware line *Output Ext Trigger Out* each time an output trigger occurs.

2.4.6.4 Output Trigger Rate Generator

The frequency of the output trigger rate generator is controlled by the RATE DIVISOR value in the Output Trigger Rate Generator control register (Table 2.4.6.4-1). With a value **Ntrig** in the register, the triggering frequency **Ftrig** is:

$$\mathbf{Ftrig} = 36,000 \div \mathbf{Ntrig},$$

where **Ftrig** is in kilohertz, and **Ntrig** can be any integer from 36 to 1048575.

2.4.7 Dynamic Function Replacement

Although access to a looping buffer is inhibited, a mechanism is provided to open the output buffer temporarily to allow a new function to replace an existing function that is circulating within the buffer. The OUTPUT ACCESS REQUEST control bit in the analog output control register, when asserted, serves as an interrupt request to the output sequencer.

When OUTPUT ACCESS REQUEST is asserted, the output sequencer waits until the EOB flag in the existing (original) function appears at the output of the buffer, and then simultaneously asserts the OUTPUT BUFFER OPEN flag and opens the buffer. The original function then begins to be flushed from the buffer, which is now open and nonlooping, and the new function can now be loaded into the buffer. When the last sample of the original function is flushed from the buffer, as indicated by the second appearance of the EOB flag, the buffer closes automatically and further access is inhibited.

If loading of the new function is completed before the old function has been completely flushed from the buffer, the new function will commence seamlessly at the clock following the last value of the original function. If however, loading of the new function is not completed in time, the buffer will close and the function will be truncated. DMA transfer rates therefore are of critical importance at high clocking rates, and a conservative typical transfer rate of 15 Megasamples per second from the host should be assumed.

2.4.8 Remote Ground Sensing

The analog outputs can be operated in a pseudo-differential mode by connecting the remote sense pin in the system I/O connector to a remote ground that is common to all output loads. To take advantage of this connection, the REMOTE SENSE control bit must be set HIGH in the BCR. To prevent extraneous interference from being introduced through the remote-sense line, the REMOTE SENSE control bit should be left in the default LOW state unless the system application specifically requires remote ground sensing.

2.4.9 Multicard Output Synchronization

If the external DAC clock inputs and outputs are interconnected between multiple cards as described in Section 3.4.2, the output channels on all of the cards can be clocked synchronously. The first card in the daisy chain is designated as the *initiator card*, and provides the clock signal for all of the other cards in the chain, designated as *target cards*.

All target cards have External Analog Output Hardware Clock selected in the OUTPUT CLOCK SOURCE field of their analog output control registers, and the initiator can be configured for any available clock source. When configured in this manner, the outputs of all target cards will clock synchronously with the outputs from the initiator.

Similarly, by daisy-chaining the DAC trigger inputs and outputs between the cards, the outputs of all target cards can be burst-synchronized to the initiator card. The target cards will have External Analog Output Hardware Trigger selected in the OUTPUT TRIGGER SOURCE fields of their analog output control registers, and the initiator card can be triggered from any available trigger source. All target cards then will initiate an output burst each time an output trigger occurs in the initiator card.

2.4.10 Range Control

The input and output voltage range is selected with the INPUT/OUTPUT RANGE control field in the BCR.

2.5 Digital Input/Output

2.5.1 Digital I/O Control Register

The ten digital I/O signals are controlled through the Digital I/O control register shown in Table 2.5.1-1. A single external output line follows the DIG AUX 01 OUTPUT control bit, and the DIG AUX 00 INPUT status bit follows a single external input line. Status bits D08-D11 are read-only flags that indicate the extent to which the digital I/O buffer is filled.

2.5.2 Bidirectional Digital Buffer

Eight bidirectional lines provide a byte-wide data port that is accessed through the Digital I/O Buffer register listed in Table 2.5.2-1. Bits D00-D07 of the buffer correspond to external digital I/O lines DIG IO 00-07 respectively, with no logic inversions. The buffer supports both single-read/write and mastered DMA transactions. Clocking of the buffer is enabled by setting the ENABLE CLOCKING control bit HIGH in the digital I/O control register. If the DIRECT I/O control bit in the digital I/O control register is HIGH, bidirectional digital I/O data bypasses the digital I/O buffer, and the clocking input is ignored.

The digital I/O buffer is organized as an 8-bit wide by 1024-byte deep FIFO, the direction of which is determined by the state of the DATA DIRECTION OUT control bit in the digital I/O control register. If the DATA DIRECTION OUT control bit is LOW, external lines DIG IO 00-07 are configured as inputs. In this case, the input of the buffer accepts input data from the external lines DIG IO 00-07, and the buffer output is available to the PCI bus. The BUFFER LOOP control bit in the digital I/O control register has no effect while the external bidirectional lines are configured as inputs.

If the DATA DIRECTION OUT control bit is HIGH, external lines DIG IO 00-07 become digital outputs, and the FIFO output is available to external lines DIG IO 00-07. If the DIRECT I/O control bit in the digital I/O control register is LOW, the input of the buffer accepts data from the PCI bus. If the BUFFER LOOP control bit in the digital I/O control register is HIGH while the port is configured as an output port, data already present in the buffer recirculates within the buffer, and write transactions from the PCIbus are ignored.

NOTE: The output of the digital I/O buffer retains either (a) the first value written to the buffer after the buffer is cleared, or (b) the last value read from the buffer. Clearing the buffer does not remove the output value, and least one clock is required to fetch a new value.

Table 2.5.2-2 summarizes the behavior of the byte-wide digital I/O port in its various operating modes. Table 2.5.2-3 lists two simple examples of typical operating sequences.

2.5.3 Digital I/O Clocking

The CLOCK SOURCE field in the digital I/O control register permits the digital I/O buffer to be clocked directly from the DIO Clock Rate Generator, or to be synchronized to the analog input or analog output clocks. Also, clocking the DIO port from the analog output trigger can provide frame-sync patterns synchronously with analog output bursts or periodic functions.

When the bidirectional digital I/O lines are configured as an output port, data from the digital I/O buffer is clocked to the system I/O connector. If the bidirectional I/O lines are configured as an input port, data from the I/O lines is clocked into the digital I/O buffer by the selected digital I/O port clock source.

2.5.4 DIO Clock Rate Generator

The frequency of this rate generator is controlled by the DIO Rate Generator control register shown in Table 2.5.4-1. With a value **Ndig** in the register, the digital I/O buffer clocking rate **Fdig** is:

$$\mathbf{Fdig} = 36 \cdot \mathbf{Ndig},$$

where **Fdig** is in megahertz, and **Ndig** can be any integer from 2 to 1048575.

NOTE: The ENABLE DIO RATE GEN control bit in the BCR must be HIGH in order to enable clocking from the DIO clock rate generator.

2.6 Interrupts

Specific events occurring within the module can be selected to produce an interrupt request on the single PCI interrupt line (INT-A). For the interrupt to be active however, it must first be enabled through the PCI adapter.

To enable interrupts from the PCI adapter:

- a. Determine the configuration address of the runtime interrupt status control register:
 - ◆ Read the PCI base address in PCI configuration space. The offset for the base address is 0x10 for memory-mapped configurations, or 0x14 for I/O-mapped configurations.
 - ◆ Add 0x68 to the base address to obtain the address of the interrupt status control register.
- b. Read the interrupt status control register, and write the value back to the register after logically OR'ing the pattern 0x0000 0900 to the value.

2.6.1 Organization

Interrupt control fields in the Interrupt Control register (Table 2.6-1) are organized into a selection field and a response field. Each available interrupt event has both a selection control bit and a corresponding response status bit. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, or by clearing the associated selection bit.

NOTE: The interrupt response status bits can only be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The PCI interrupt output from the module is asserted if any response bit in the interrupt control register is asserted (and if the interrupt is enabled in the PCI adapter). To clear the interrupt, all response bits must be cleared.

2.6.2 Event Detection

Interrupt event detection is edge-activated on a transition of the selected event from false to true. Once asserted, each response status bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

2.7 Direct Memory Access

For those registers that support DMA, PCI data transfers are executed with the module acting as DMA master. The typical local configuration registers listed in Table 2.7-1 control the DMA configuration for data transfers both to and from the module.

2.8 Autocalibration

To ensure full conformance with the product specification, autocalibration should always be invoked after power has been applied to the board and the system has reached thermal equilibrium, or after a software or hardware reset has occurred. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs immediately after power is applied. The autocalibration process is independent of all control parameters, and all input and output channels are calibrated regardless of which channels are designated as active or inactive.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration, which has a duration of approximately 4-8 seconds, is indicated by the AUTOCAL bit clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event. Read/write accesses from the PCI bus during autocalibration can produce unpredictable results, and are not recommended. The software-controlled board configuration that exists when autocalibration is invoked is restored when autocalibration has been completed.

The autocalibration process may be unable to successfully calibrate all analog channels if a board is marginal or defective. Should this situation occur, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS after autocalibration indicates that the calibration was successful.

2.9 Analog Output Control Sequence Examples

This section provides general descriptions of typical control sequences for producing the following operating modes. These examples represent only a few of many possible applications:

Direct Output:	Data written to the analog output buffer is clocked immediately to the outputs.
Continuous Function, Nonlooping:	Streaming mode. Data flows through the buffer to the outputs.
Continuous Function, Looping:	Periodic Continuous Function. The function is retained in the buffer, and is clocked continuously to the outputs.
Burst Function, Looping:	Periodic One-Shot function. Clocking is initiated by a trigger, after which the function is clocked to the outputs and then terminates until another trigger occurs. The function remains in the buffer, and can be triggered repeatedly.
Dynamic Function Replacement:	An currently clocking function in a looping (closed) buffer is replaced seamlessly by a new function.

Each example can be applied to either buffer, and assumes that the following parameters have already been selected:

Parameter	Reference Section
Channel Selection	2.4.2
Buffer Threshold; if required	2.4.4.2
Clock Source	2.4.5.1
Clocking Rate: (If the output rate generator is the selected clocking source)	2.4.5.4
Clocking Mode; Simultaneous or Sequential	2.4.5.3

2.9.1 Direct Output

- a. Enable clocking.
- b. Write a sequence of sample values to the analog output buffer (2.4.4). If *simultaneous sampling* is selected, all samples in each scan appear simultaneously at the outputs when each clock occurs.

If *sequential clocking* is selected, each sample appears individually at its associated output when an output clock occurs.

2.9.2 Continuous Function, Nonlooping

This operating mode is similar to the Direct Output mode, but the output buffer is not allowed to become empty, and the output is a continuous sequence of sample values.

- a. Enable clocking (2.4.5.2). Alternatively, enabling of the clock can be delayed until an initial block of sample values has been written to the buffer.
- b. Commence writing a sequence of sample values to the buffer (2.4.4). Using the buffer threshold flag (2.4.4.2), ensure that the buffer becomes neither empty nor full.
- c. The active outputs receive new values from the buffer continuously until the input data stream to the buffer terminates. When data input from the PCIbus ceases, the data samples remaining in the buffer continue to be clocked to the outputs until the buffer becomes empty.

2.9.3 Continuous Function, Looping

- a. Write an entire function or sequence of sample values to the buffer (2.4.4).
- b. Select the looping mode (2.4.4.5). Subsequent values written to the buffer are ignored.
- c. Enable clocking (2.4.5.2).
- d. The active outputs receive new values from the buffer continuously until clocking is disabled. The function is retained indefinitely, and circulates continuously within the buffer.

2.9.4 Burst Function, Looping

- a. Write an entire function or sequence of values to the buffer (2.4.4). Attach the END OF BURST flag to the last value in the function (2.4.4.5).
- b. Select the looping mode (2.4.4.5). Subsequent values written to the buffer are ignored.
- c. Select a burst triggering source (2.4.6.3). Selection of a burst trigger source automatically enables the burst triggering mode.
- d. Select the trigger rate if the trigger source is the output rate generator (2.4.5.4).
- e. Enable clocking (2.4.5.2).
- f. Clocking commences when the first trigger occurs, and terminates when the last value in the function has been clocked to the outputs. The function is retained indefinitely within the buffer, and each subsequent trigger initiates the function again.

2.9.5 Dynamic Function Replacement

- a. Initiate a continuous looping function, as described above in 2.9.3, but attach an END OF BURST tag (Buffer bit D16) to the last value in the function.

Note: Do not select a burst triggering mode. The EOB tag is used here only to identify the end of the function.

- b. Set the OUTPUT ACCESS REQUEST flag HIGH in the buffer control register, and wait for the OUTPUT BUFFER OPEN flag to be asserted HIGH.
- c. Load a new function into the buffer *while the OUTPUT BUFFER OPEN flag is HIGH*. (The flag will go LOW again when the last value of the original function is clocked from the buffer). Attach an EOB flag to the last value of the new function.

Note: Do not clear the OUTPUT ACCESS REQUEST flag, or the buffer may close prematurely. The request flag is cleared automatically when the last value of the original function is clocked from the buffer.

- d. The remainder of the original function clocks to the outputs, after which the buffer closes and the new function seamlessly begins clocking to the outputs and circulating within the buffer.

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2.9 Control Section Tables

Table 2.1-1. Local Control Registers

LOCAL ADDR	ACCESS MODE	REGISTER	DEFAULT	FUNCTION
0x00	RW	BOARD CONTROL	0x0002 0006	Board Control Register (BCR)
0x04	RW	CHANNEL-ENABLE MASKS	0x0000 0F0F	Enabling mask for analog inputs and outputs
0x08	RO (DMA)	ANALOG INPUT BUFFER	0xXXXX XXXX	Analog Input data
0x0C	RW	INPUT BUFFER HIGH THRESHOLD	0x0000 D000	Input Buffer-flag high threshold
0x10	RW	INPUT BUFFER LOW THRESHOLD	0x0000 3000	Input Buffer-flag low threshold
0x14	RW	ANALOG INPUT CONTROL	0x0000 0001	Analog Inputs control register
0x18	WO (DMA)	ANALOG OUTPUT BUFFER	---	Analog Output data
0x1C	RW	OUTPUT BUFFER HIGH THRESHOLD	0x0000 D000	Output buffer-flag high threshold
0x20	RW	OUTPUT BUFFER LOW THRESHOLD	0x0000 3000	Output buffer-flag low threshold
0x24	RW	ANALOG OUTPUT CONTROL	0x0000 0401	Analog Outputs control register
0x28	RW (DMA)	DIGITAL I/O BUFFER	0x0000 00XX	Bidirectional digital I/O data FIFO buffer
0x2C	R/W	DIGITAL I/O CONTROL	0x0000 0X10	Digital I/O control register
0x30	R/W	INPUT CLOCK RATE GENERATOR	0x0000 0032	Analog input clocking rate divisor
0x34	R/W	INPUT TRIGGER RATE GENERATOR	0x0000 0168	Analog Input trigger rate divisor
0x38	R/W	OUTPUT CLOCK RATE GENERATOR	0x0000 0032	Analog Output clocking rate divisor
0x3C	R/W	OUTPUT TRIGGER RATE GENERATOR	0x0000 0168	Analog Output trigger rate divisor
0x40	R/W	DIO CLOCK RATE GENERATOR	0x0000 0002	Digital I/O clocking rate divisor
0x44	RW	INTERRUPT CONTROL	0x0000 0000	Interrupt event selection and status
0x48	RW	INPUT BURST SIZE	0x0000 0100	Number of analog input samples in a triggered burst.
0x4C	RO	F/W Revision *	---	*
0x50	RO	Autocalibration Values *	---	*
0x54-0x7F	RO	(Reserved)	---	(Inactive)

RW = Read/Write; RO = Read-Only; WO = Write-Only; X = Undefined state.

* Test registers; shown for reference only.

Table 2.1-2. Board Control Register; Offset 0x00; Default 0x0002 0006

DATA BIT	DESIGNATION	DEFAULT	DESCRIPTION
D00-D01	INPUT/OUTPUT RANGE	2	Controls the input and output voltage range as: Code Range ----- 0 ±2.5V 1 ±5V 2 ±10V 3 (Reserved)
D02	OFFSET BINARY DATA	1	Selects two's complement output data format when LOW, or offset binary format when HIGH.
D03 *	INPUT BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in the Analog Input Buffer is greater than the Input Buffer LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the Analog Input control register.
D04 *	OUTPUT BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in the Analog Output Buffer is greater than the Output Buffer LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the Analog Output control register.
D05 **	CLEAR ANALOG OUTPUT BUFFER	0	Clears the analog output buffer and sequencer
D06 **	CLEAR ANALOG INPUT BUFFER	0	Clears the analog input buffer and sequencer
D07 **	CLEAR DIGITAL I/O BUFFER	0	Clears the digital I/O buffer and sequencer
D08	ENABLE INPUT CLOCK RATE GEN	0	Enables analog input clocking
D09	ENABLE OUTPUT CLOCK RATE GEN	0	Enables analog output clocking
D10	ENABLE INPUT CLOCKING	0	Enables analog input clocking
D11	ENABLE OUTPUT CLOCKING	0	Enables analog output clocking
D12	ENABLE INPUT TRIGGERING	0	Enables analog output triggering. Ignored for continuous clocking
D13	ENABLE OUTPUT TRIGGERING	0	Enables analog input triggering. Ignored for continuous clocking.
D14	ENABLE DIO RATE GEN	0	Enables the digital I/O rate generator
D15	(Reserved)	0	---
D16 **	AUTOCAL	0	Initiates an autocalibration operation.
D17 *	AUTOCAL PASS	1	Indicates a successful autocalibration when HIGH, or a failure when LOW.
D18	REMOTE SENSE	0	Enables remote ground sensing for analog outputs.
D19 **	INITIALIZE BOARD	0	Initializes the board. Sets all defaults.
D20-31 *	(Reserved)	0x0	Read-only. Returns all-zero value.

* Read-Only. All other bits are Read/Write. ** Control bit clears automatically upon completion.

Table 2.3.2.1-1. Channel-Enable Mask Register; Offset 0x04; Default 0x0000 0F0F

DATA BIT	DESIGNATION	DEF	DESCRIPTION
D00	ENABLE INPUT CHAN 00	1	Analog input channel-enable mask. An input is enabled if the associated mask bit is HIGH.
D01	ENABLE INPUT CHAN 01	1	
D02	ENABLE INPUT CHAN 02 **	1	
D03	ENABLE INPUT CHAN 03 **	1	
D04-07 *	(Reserved)	0	Read-only. Returns all-zero value.
D08	ENABLE OUTPUT CHAN 00	1	Analog output channel-enable mask. An output is enabled if the associated mask bit is HIGH
D09	ENABLE OUTPUT CHAN 01	1	
D10	ENABLE OUTPUT CHAN 02 **	1	
D11	ENABLE OUTPUT CHAN 03 **	1	
D04-31 *	(Reserved)	0	Read-only. Returns all-zero value.

* Read-only. All other control bits are read/write.

** 8-Channel configuration only. Ignored in 4-Channel configuration.

Table 2.3.3-1. Analog Input Control Register; Offset: 0x14; Default: 0x0000 0001

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-01	R/W	INPUT CLOCK SOURCE	1	Selects and enables the Analog Input clocking source: Code Analog Input Clocking Source ----- 0 Software Clcking Enabled 1 Analog Input Clock Rate Generator 2 (Reserved) 3 External Analog Input Hardware Clock
D02	RO	READY FOR INPUT CLOCK	0	When HIGH, indicates that an analog input software clock will be accepted by if software clocking is selected for the INPUT CLOCK SOURCE.
D03	R/W	ANALOG INPUT SOFTWARE CLOCK *	0	D07 (Reserved)
D04-05	R/W	INPUT TRIGGER SOURCE	0	Selects and enables the Analog Input burst trigger source: Code Analog Input Burst Trigger Source ----- 0 Continuous Operation. Trigger Disabled 1 Analog Input Trigger Rate Generator 2 (Reserved) 3 External Analog Input Hardware Trigger
D06	RO	READY FOR INPUT TRIGGER	0	When HIGH, indicates that an analog input software trigger will be accepted if input triggering is enabled.
D07	R/W	INPUT SOFTWARE TRIGGER *	0	Produces a single analog input trigger when asserted, if input triggering is enabled and READY FOR INPUT TRIGGER is HIGH. Software triggering is enabled in all input triggering modes except Continuous Operation.
D08	R/W	SEQUENCED SAMPLING	0	When this bit is LOW, all active inputs are clocked simultaneously. Setting this bit HIGH causes even/odd input pairs to clock on alternate input clocks. Even channels are sampled first, odd channels last.
D09-10	R/W	(Reserved)	0	---
D11	R/W	CLEAR ANALOG OUTPUT BUFFER *	0	Resets the analog input buffer to empty. Duplicated in the BCR.
D12	R/W	WARP MODE	0	Selects the ADC's warp mode, in which the minimum delay between samples is 1ms.
D13	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in the analog input buffer is greater than the Input Buffer LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the board control register.
D14-31	RO	(Reserved)	0	Read-only. Returns all-zero value.

R/W = Read/Write, RO = Read-only.

* Clears LOW automatically when operation is completed.

Table 2.3.4-1. Analog Input Buffer Register; Offset: 0x08

DATA BIT	DESIGNATION	FUNCTION
D00-15	INPUT DATA	16-bit analog input data
D16	END OF BURST (EOB)	EOB: Indicates the last value of a burst.
D17	EVEN CHANNEL	Asserted HIGH for even-numbered analog input channels. I.e.: Channels 00, 02.
D18-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.4.2-1. Input Buffer Threshold Registers

HIGH Threshold: Offset: 0x0C; Default: 0x0000 D000
LOW Threshold: Offset: 0x10; Default: 0x0000 3000

DATA BIT	DESIGNATION	FUNCTION
D00-15	BUFFER THRESHOLD	16-Bit buffer HIGH or LOW threshold value. The associated buffer threshold flag is asserted HIGH when buffer contents are greater than the LOW threshold, and less than or equal to the HIGH threshold.
D16-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.5.3-1. Input Clock Rate Generator Control

Offset: 0x30; Default: 0x0000 0032

DATA BIT	DESIGNATION	FUNCTION
D00-15	RATE DIVISOR	Analog Input rate generator divisor
D16-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.3.6.4-1 Input Trigger Rate Generator Control

Offset: 0x34; Default: 0x0000 0168

DATA BIT	DESIGNATION	FUNCTION
D00-19	RATE DIVISOR	Output trigger rate generator divisor
D20-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.4.3-1. Analog Output Control Register; Offset: 0x24; Default: 0x0000 0401

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-01	R/W	OUTPUT CLOCK SOURCE	1	Selects and enables the Analog Output clocking source: Code Analog Output Clocking Source ----- 0 Software Cloning Enabled 1 Analog Output Clock Rate Generator 2 Analog Input Clock 3 External Analog Output Hardware Clock
D02	RO	READY FOR OUTPUT CLOCK	0	When HIGH, indicates that an analog output software clock will be accepted by if software cloning is selected for the OUTPUT CLOCK SOURCE.
D03	R/W	OUTPUT SOFTWARE CLOCK*	0	Produces a single analog output clock when asserted, if software cloning is enabled and READY FOR OUTPUT CLOCK is HIGH.
D04-05	R/W	OUTPUT TRIGGER SOURCE	0	Selects and enables the Analog Output burst trigger source: Code Analog Output Burst Trigger Source ----- 0 Continuous Operation. Trigger Disabled 1 Analog Output Trigger Rate Generator 2 Analog Input Trigger 3 External Analog Output Hardware Trigger
D06	RO	READY FOR OUTPUT TRIGGER	0	When HIGH, indicates that an analog output software trigger will be accepted if output triggering is enabled.
D07	R/W	OUTPUT SOFTWARE TRIGGER*	0	Produces a single analog output trigger when asserted, if output triggering is enabled and READY FOR OUTPUT TRIGGER is HIGH. Software triggering is enabled in all output triggering modes except Continuous Operation.
D08	R/W	OUTPUT LOOPING	0	When HIGH, selects analog output buffer looping. Disables PCIbus access to the buffer unless ACCESS REQUEST is asserted.
D09	R/W	OUTPUT ACCESS REQUEST*	0	Requests access to a looping (closed) analog output buffer when HIGH. Accessibility is indicated by the OUTPUT BUFFER OPEN flag.
D10	RO	OUTPUT BUFFER OPEN	1	When HIGH, indicates that the analog output buffer will accept data.
D11	R/W	CLEAR ANALOG OUTPUT BUFFER*	0	Resets the analog output buffer to empty. Duplicated in the BCR.
D12	R/W	SEQUENTIAL OUTPUT CLOCKING	0	Selects analog output sequential clocking when HIGH, or simultaneous clocking when LOW.
D13	RO	BUFFER THRESHOLD FLAG	0	Asserted HIGH when the number of values in the analog output buffer is greater than the Output Buffer LOW threshold, and less than or equal to the HIGH threshold. Duplicated in the board control register..
D14-31	RO	(Reserved)	0	Read-only. Returns all-zero value.

R/W = Read/Write, RO = Read-only.

* Clears LOW automatically when operation is completed.

Table 2.4.4-1. Analog Output Buffer Register; Offset: 0x18

DATA BIT	DESIGNATION	FUNCTION
D00-15	OUTPUT DATA *	16-bit analog output data
D16	END OF BURST (EOB)	EOB: Indicates the end of a burst function. Principal purpose is the termination of a burst.
D17	RATE CHANGE	New Clocking Rate-A: The OUTPUT DATA field replaces the Rate Control-A register for frequency control.
D18-31	(Reserved)	Read-only. Returns all-zero value.

* Context changes to "Rate Generator Divisor" if RATE CHANGE is HIGH.

Table 2.4.4.2-1. Output Buffer Threshold Registers

HIGH Threshold: Offset: 0x1C; Default: 0x0000 D000
LOW Threshold: Offset: 0x20, Default: 0x0000 3000

DATA BIT	DESIGNATION	FUNCTION
D00-15	BUFFER THRESHOLD	16-Bit buffer HIGH or LOW threshold value. The associated buffer threshold flag is asserted HIGH when buffer contents are greater than the LOW threshold, and less than or equal to the HIGH threshold.
D16-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.4.5.4.1-1. Output Clock Rate Generator Control

Offset: 0x38; Default: 0x0000 0032 *

DATA BIT	DESIGNATION	FUNCTION
D00-15	RATE DIVISOR	Analog Output rate generator divisor
D16-31	(Reserved)	Read-only. Returns all-zero value.

* The frequency of the output clock rate generator can be controlled also through the analog output data buffer.

Table 2.4.6.4-1 Output Trigger Rate Generator Control

Offset: 0x3C; Default: 0x0000 0168

DATA BIT	DESIGNATION	FUNCTION
D00-19	RATE DIVISOR	Output trigger rate generator divisor
D20-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.5.1-1. Digital I/O Control Register; Offset 0x2C; Default 0x0000 0X10

BITS	DESIGNATION	DEFAULT	FUNCTION *
D00	DATA DIRECTION OUT	0	Configures the bidirectional data lines as outputs from D00-07 of this register when asserted HIGH, or as inputs to this register when LOW.
D01	BUFFER LOOP	0	Closes the buffer for data recirculation when HIGH, opens the buffer for pass-thru operation when LOW.
D02	CLEAR DIGITAL BUFFER	0	Clears the digital I/O buffer. (Bit clears automatically). Duplicated in the BCR.
D03	ENABLE CLOCKING	0	Enables digital I/O buffer clocking from Rate Generator-D
D04	DIRECT I/O	1	Routes I/O data around (bypasses) the digital I/O FIFO
D05	(Reserved)	---	---
D06	DIG AUX 01 OUTPUT	0	Output-only digital line
D07	DIG AUX 00 INPUT	X	Read-Only. Input-only digital line
D08	BUFFER EMPTY	1	Read-Only. HIGH only when the digital buffer is empty.
D09	BUFFER 1/4 FULL	0	Read-Only. HIGH when the buffer is 1/4 full or more.
D10	BUFFER 3/4 FULL	0	Read-Only. HIGH when the buffer is 3/4 full or more.
D11	BUFFER FULL	0	Read-Only. HIGH only when the buffer is full.
D12-13	CLOCK SOURCE	0	Selects and enables the Digital I/O port clocking source: Code Digital I/O Clocking Source ----- 0 Rate-DIO Generator 1 Analog Input Clock 2 Analog Output Clock 3 Analog Output Trigger
D14-31	(Reserved)	---	Read-only. Returns all-zero value.

* All control bits are READ/WRITE unless indicated otherwise

Table 2.5.2-1. Digital I/O Buffer Register; Offset: 0x28

DATA BIT	DESIGNATION	FUNCTION
D00-07	DIGITAL I/O DATA	Bidirectional digital I/O data FIFO
D08-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.5.2-2. Digital I/O Buffer Activity Modes

DATA DIRECTION	PCibus TRANSACTION	BUFFER LOOP	DIRECT I/O	DATA ACTIVITY
INPUT	READ	Don't Care	LOW	PCibus reads the digital I/O FIFO.
INPUT	READ	Don't Care	HIGH	DIRECT-READ MODE: (Default) PCibus reads directly from the external digital I/O lines
INPUT	WRITE	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus data is ignored.
OUTPUT	WRITE	Don't Care	HIGH	DIRECT-WRITE MODE: PCibus writes directly to the external digital I/O lines.
OUTPUT	WRITE	LOW	LOW	PASSTHRU MODE: PCibus writes to the digital I/O FIFO. External digital I/O lines follow the FIFO output.
OUTPUT	WRITE	HIGH	LOW	RECIRCULATION MODE (Looping): PCibus data is ignored. Data already present in the FIFO recirculates. External digital I/O lines follow the FIFO output.
OUTPUT	READ	Don't Care	Don't Care	(Invalid Operation): Digital I/O FIFO is unaffected. PCibus reads the previous value written to the port.

Table 2.5.2-3. Typical Digital I/O Operation

CLOCKED OUTPUT PORT		CLOCKED INPUT PORT	
STEP	OPERATION	STEP	OPERATION
1 *	Configure as an output port. (DATA DIRECTION OUT = HIGH) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)	1 *	Configure as an input port. (DATA DIRECTION OUT = LOW) Disable digital clocking (ENABLE CLOCKING = LOW) Clear the digital I/O buffer. (CLEAR DIGITAL BUFFER = HIGH) Select clocking mode. (DIRECT IO = LOW)
2	Load the buffer with a pattern sequence.	2	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)
3	Adjust the I/O rate generator to the required clocking rate. (Not required for direct I/O)	3	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)
4	Enable digital I/O clocking. ** (ENABLE CLOCKING = HIGH)	4	The buffer begins to fill with data from the digital I/O port.
5	Data from the buffer begins to clock to the digital I/O port. If looping has not been selected, the buffer accepts subsequent data from the PCI bus.		

* Adjust all digital I/O control register bits simultaneously.

** Do not clear the buffer again at this point. For looping (periodic function generation), set BUFFER LOOP = HIGH.

Table 2.5.4-1. DIO Rate Generator Control Register
Offset: 0x40; Default: 0x0000 0002

DATA BIT	DESIGNATION	FUNCTION
D00-19	RATE DIVISOR	Rate generator divisor for master clock
D20-31	(Reserved)	Read-only. Returns all-zero value.

Table 2.6-1 Interrupt Control Register; Offset 0x44; Default 0x0000 0000

CONTROL BITS	INTERRUPT EVENT	FUNCTION
D00	Initialization completed	Interrupt event selection. Enables assertion of the corresponding event flag (below) when the selected event occurs.
D01	Autocal completed	
D02	Input Buffer threshold flag HIGH-to-LOW transition	
D03	Output Buffer threshold flag HIGH-to-LOW transition	
D04	(Reserved)	
D05	(Reserved)	
D06	Digital buffer 1/4-Full HIGH-to-LOW transition	
D07	Digital buffer 3/4-Full LOW-to-HIGH transition	
D08	Initialization completed	Interrupt response. Asserted HIGH when a selected interrupt (above) occurs. Remains HIGH until cleared LOW. The PCI bus INT A interrupt is asserted while any event flag in this register is asserted.
D09	Autocal completed	
D10	Input Buffer threshold flag HIGH-to-LOW transition	
D11	Output Buffer threshold flag HIGH-to-LOW transition	
D12	(Reserved)	
D13	(Reserved)	
D14	Digital buffer 1/4-Full HIGH-to-LOW transition	
D15	Digital buffer 3/4-Full LOW-to-HIGH transition	
D16-31	(Reserved)	

Table 2.7-1. Typical DMA Control Registers

CONFIGURATION REGISTER	OFFSET*	DMA FUNCTION	COMMENTS and TYPICAL VALUES
PCI Status and Command	0x04	Bus mastering selection.	Logically OR 0x0004 for bus mastering.
DMA-0 Mode	0x80	32-Bit bus, Interrupt on done, nonincrementing, local bursting, DMA Chan-0	0x0002 0D43
DMA-0 PCI Address	0x84	Initial PCI data address	Application-dependent
DMA-0 Local Address	0x88	Initial local address	Local address of data register (Table 2.1-1)
DMA -0 Transfer Byte Count	0x8C	Number of bytes in transfer	Application-dependent
DMA Descriptor Counter	0x90	Transfer direction	0x0000 0000, PCI to card (write) 0x0000 000A, Card to PCI (read)
DMA-0 Command Status	0xA8	Enable/initiate transfer	0x0000 0001 to enable transfer 0x0000 0003 to initiate transfer

* From base address.

SECTION 3.0 HARDWARE INSTALLATION

3.1 System Configuration

A typical installation of a PMC I/O module involves several fundamental tasks, namely:

- ◆ Configuration of the PMC module
- ◆ System cabling and connections
- ◆ Physical installation of the PMC module on the PMC host board
- ◆ Maintenance.

The configuration of the PMC-2215 is established at the factory, and no electrical modifications are required in the field. This section provides specific information and guidelines pertaining to the remaining installation tasks. Contact Sales at Rymic Systems if prewired or custom cable assemblies are required.

3.1.1 I/O Connections

Pin assignments for the System Input/Output connector are tabulated in Table 3.1.1-1 located at the end of this section. Figure 3.1.1-1 shows the physical arrangement of the connector, which is a 68-Pin 2-Row 0.050-inch subminiature connector that is designed to mate with Robinson-Nugent Model P50E-068-S-TG or equivalent cable socket connector. Unused pins can be left disconnected in most applications, but grounding of the unused analog inputs and the GROUND SENSE input line to ANA RTN can minimize the injection of noise into the card when operating in high-noise environments.

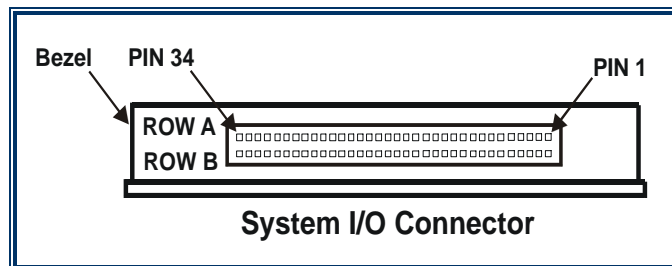


Figure 3.1.1-1. System I/O Connector

3.1.2 System Cabling

If discrete-wire system cabling is used, analog input pairs lines should be arranged into twisted pairs, with the HI and LO lines of each channel twisted together. Likewise, each analog output OUT line should be twisted with an OUT RTN line. If ribbon cable is used, the wire sequence is automatically ordered to ensure that the correct wire pairs are twisted together within the cable.

3.2 Analog Inputs

The four analog input channels can be configured as all differential or as all single-ended inputs. The differential/single-ended configuration must be implemented in both the input wiring and the control software.

Differential operation can be used for either floating or grounded signal sources, as long as the maximum common-mode input voltage (CMV) does not exceed the specified common mode input voltage. Differential inputs provide the maximum immunity to noise, crosstalk and ground loops, and are recommended when system wiring permits this configuration.

Single-ended inputs should be used only when the input signal sources either are isolated from each other, or share a common return that is isolated from system ground. Single-ended inputs are especially susceptible to errors and noise introduced by system ground loops and cabling.

Table 3.2-1 lists the most common connections for differential and single-ended input configurations.

3.3 Analog Outputs

All four analog output channels are single-ended, and are intended to drive floating loads, or loads that are common to a ground point that is within ± 1 -Volt of the PCI bus ground.

For loads that are not floating but that have a common ground point, connecting the GROUND SENSE input to the common ground can reduce errors from a potential on the remote ground. Remote sensing must be enabled through the application software in order to implement this connection.

Note: The GROUND SENSE input will correct for DC offsets between grounds, but will not reject high-frequency ground noise.

Consideration should be given to the voltage drop in the output and return lines when operating into significant loads. For example, a 1-milliamp load will produce a line drop of approximately 60 μ V per foot in #28 AWG copper wire. Even in a relatively short cable, this drop could be significant when using a ± 2.5 V output range, for which 1-LSB is equivalent to 76 μ V.

3.4 External Clocks and Triggers

External clocking and burst triggering can be implemented in system wiring and the control software. If either or both of these features are to be implemented, the card must be wired accordingly. The following descriptions apply equally to both analog input (ADC) and analog output (DAC) clocking and triggering.

3.4.1 Clock and Trigger Inputs

To connect the card for external clocking, connect the external clock source to the ADC/DAC CLOCK INPUT pin, and the clock source return to DIG RTN. Similarly, for external burst triggering, connect the trigger source to the ADC/DAC TRIG INPUT pin. The CLOCK and TRIG inputs accept standard TTL levels, and provide an internal 4.7K pullup resistance to +5 Volts. Both inputs are active on the falling (LOW) edges of the input signals.

3.4.2 Multicard Clocking and Burst Triggering

3.4.2.1 Analog Inputs

For multicard synchronous analog input sampling, one of the cards is designated as the **initiator**, and the remaining cards are designated as **targets**. If external clock and trigger sources are to be used, the clock and trigger inputs for the initiator are connected as described in Paragraph 3.4.1. If external signals are not required, the clock and trigger input connections at the initiator can be left disconnected.

The ADC CLOCK OUTPUT signal from the initiator is connected to the ADC CLOCK INPUT pin of one of the target cards, designated as Target-1. If more than one target card is present, the ADC CLOCK OUTPUT from Target-1 is connected to the ADC CLOCK INPUT pin of TARGET-2, and this sequence is repeated for all remaining target cards. The ADC CLOCK OUTPUT from the last target in the chain is not connected.

For multicard synchronous analog input triggering, the ADC TRIG OUTPUT and ADC TRIG INPUT connections between cards are configured as described above for synchronous output clocking.

3.4.2.2 Analog Outputs

Synchronization of the analog outputs on multiple cards is identical to the synchronization of analog inputs described in Section 3.4.2.1, with DAC clock and trigger signals replacing the corresponding ADC signals.

3.5 Digital Input/Output

Digital lines DIG IO 00 through DIG IO 07 are bidirectional, with the signal direction controlled by the control software. DIG AUX 00 is a digital input-only pin, and DIG AUX 01 is a digital output-only pin. DIG AUX 00 and DIG IO 00 through DIG IO 07 are provided with internal 4.7K pullup resistors to +5 Volts. All ten digital lines are compatible with standard TTL levels.

3.6 Physical Installation

Before removing the PMC module from the protective antistatic shipping envelope, ensure that the host board on which the module is to be installed is ready to receive the module. The host panel opening and the mating mezzanine connectors should be free of obstructions such as protective covers and filler panels. After removing the PMC module from the antistatic shipping envelope, remove and save any mounting screws that may be installed in the bezel and standoffs.

Position the PMC module above the host as shown in Figure 3.6-1, with the PCI mezzanine connectors facing the host board, and with the I/O connector and bezel oriented toward the front panel of the host. Carefully insert the bezel of the module through the appropriate opening in the host panel, and align the PCI mezzanine connectors at the rear of the module with the mating connectors on the host.

Press the rear of the module carefully but firmly downward onto the host until the bezel and the standoffs are seated against the host board. Verify that the PCI connectors have mated correctly.

Install the four 2.5mm mounting screws supplied with the module, through the host board and into the bezel and the two standoffs on the module. This completes the physical installation of the PMC module.

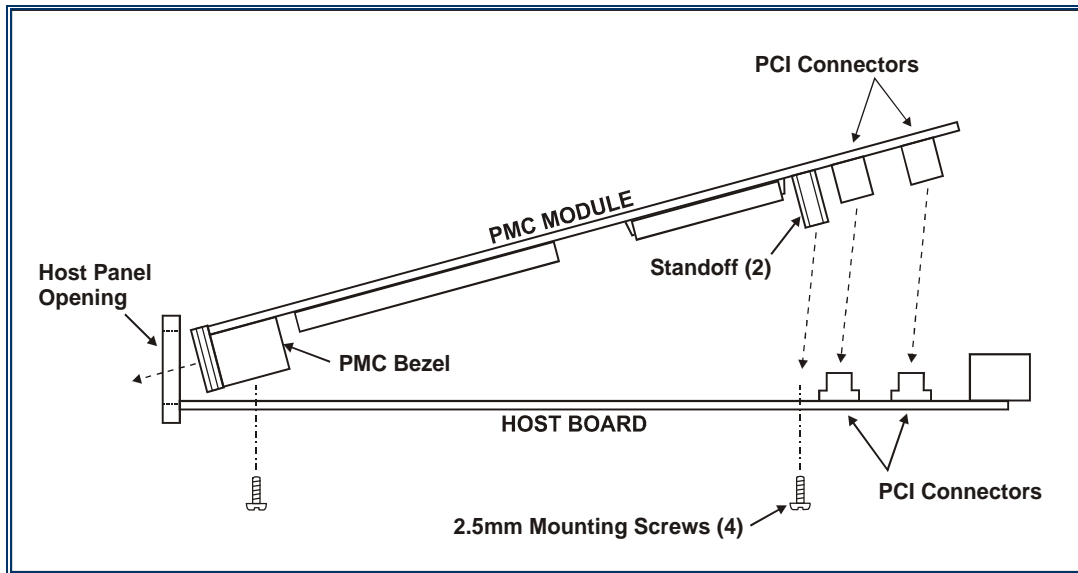


Figure 3.6-1. Physical Installation

3.7 Maintenance

Aside from the usual care associated with precision electronic equipment, this product requires no scheduled maintenance. In environments that contain high levels of dust, smoke or other airborne particulate materials, the module should be cleaned periodically to prevent the accumulation of surface deposits that can reduce the ability of power components to dissipate heat.

3.8 Internal Reference Test Point

The internal calibration reference that is used to calibrate all analog input and output channels during autocalibration is available between the TEST OUT(+) and TEST OUT(-) pins of the I/O connector. Under normal conditions, this reference should not require adjustment. However, if module accuracy appears to degrade, verify that the voltage between these pins conforms to Table 3.8-1. If adjustment is required, adjust the reference trimmer located at the edge of the board until the measured voltage conforms to Table 3.8-1.

Table 3.1.1-1. System I/O Connector Pin Functions

PIN	FUNCTION	PIN	FUNCTION
1A	DIG RTN	1B	DIG RTN
2A	ADC TRIG INPUT	2B	ADC TRIG OUTPUT
3A	DIG RTN	3B	DIG RTN
4A	ADC CLOCK INPUT	4B	ADC CLOCK OUTPUT
5A	DIG RTN	5B	DIG RTN
6A	DAC TRIG INPUT	6B	DAC TRIG OUTPUT
7A	DIG RTN	7B	DIG RTN
8A	DAC CLOCK INPUT	8B	DAC CLOCK OUTPUT
9A	OUT RTN	9B	DIG RTN
10A	GROUND SENSE	10B	DIG IO 00
11A	OUT RTN	11B	DIG RTN
12A	ANA OUT 00	12B	DIG IO 01
13A	OUT RTN	13B	DIG RTN
14A	ANA OUT 01	14B	DIG IO 02
15A	OUT RTN	15B	DIG RTN
16A	ANA OUT 02 *	16B	DIG IO 03
17A	OUT RTN	17B	DIG RTN
18A	ANA OUT 03 *	18B	DIG IO 04
19A	INP RTN	19B	DIG RTN
20A	INP RTN	20B	DIG IO 05
21A	ANA INP LO 00	21B	DIG RTN
22A	ANA INP HI 00	22B	DIG IO 06
23A	INP RTN	23B	DIG RTN
24A	INP RTN	24B	DIG IO 07
25A	ANA INP LO 01	25B	DIG RTN
26A	ANA INP HI 01	26B	DIG AUX 01 (Input)
27A	INP RTN	27B	DIG RTN
28A	INP RTN	28B	DIG AUX 02
29A	ANA INP LO 02 *	29B	DIG RTN
30A	ANA INP HI 02 *	30B	DIG RTN
31A	INP RTN	31B	INP RTN
32A	INP RTN	32B	INP RTN
33A	ANA INP LO 03 *	33B	TEST OUT(-)
34A	ANA INP HI 03 *	34B	TEST OUT(+)

* 8-Channel configuration only.

Table 3.2-1. Analog Input Connections

DIFFERENTIAL INPUTS		SINGLE-ENDED INPUTS	
CONNECT	TO	CONNECT	TO
ANA INP HI xx	Input device output (+)	ANA INP HI xx	Input Device output
ANA INP LO xx	Input device return (-)	ANA INP HI xx	(Not Connected)
INP RTN	Remote Ground/Return	INP RTN	Remote Ground/Return

"xx" = Input channel number

Table 3.8-1. Internal Reference Voltage

FULLSCALE RANGE	INTERNAL REFERENCE VOLTAGE
±2.5V	+2.4988V ±0.0004V
±5V	+4.9975V ±0.0005V
±10V	+9.9950V ±0.0007V

SECTION 4.0 FUNCTIONAL DESCRIPTION

4.1 External Interfaces

Two electrical interfaces provide connections between the PMC-2215 module and external system components. The host board controls the module through two PCI bus connectors that mate with two corresponding connectors located on the host (Figure 4.1-1). These connectors provide a standard 32-bit, 33 MHz PCI control interface that conforms to the IEEE PCI local bus specification Revision 2.2. The host interface also supplies +5 VDC power for the module, and exchanges output data and control/status information with the host.

A system input/output connector supplies the second electrical interface, which provides connections to system signals that are external to both the host and the host assembly. The I/O connector is located in an access opening in the front panel of the host board, and is designed to interface electrically and mechanically with conventional system cabling. All analog inputs and outputs, digital I/O signals and external clock and trigger signals pass through the system I/O connector.

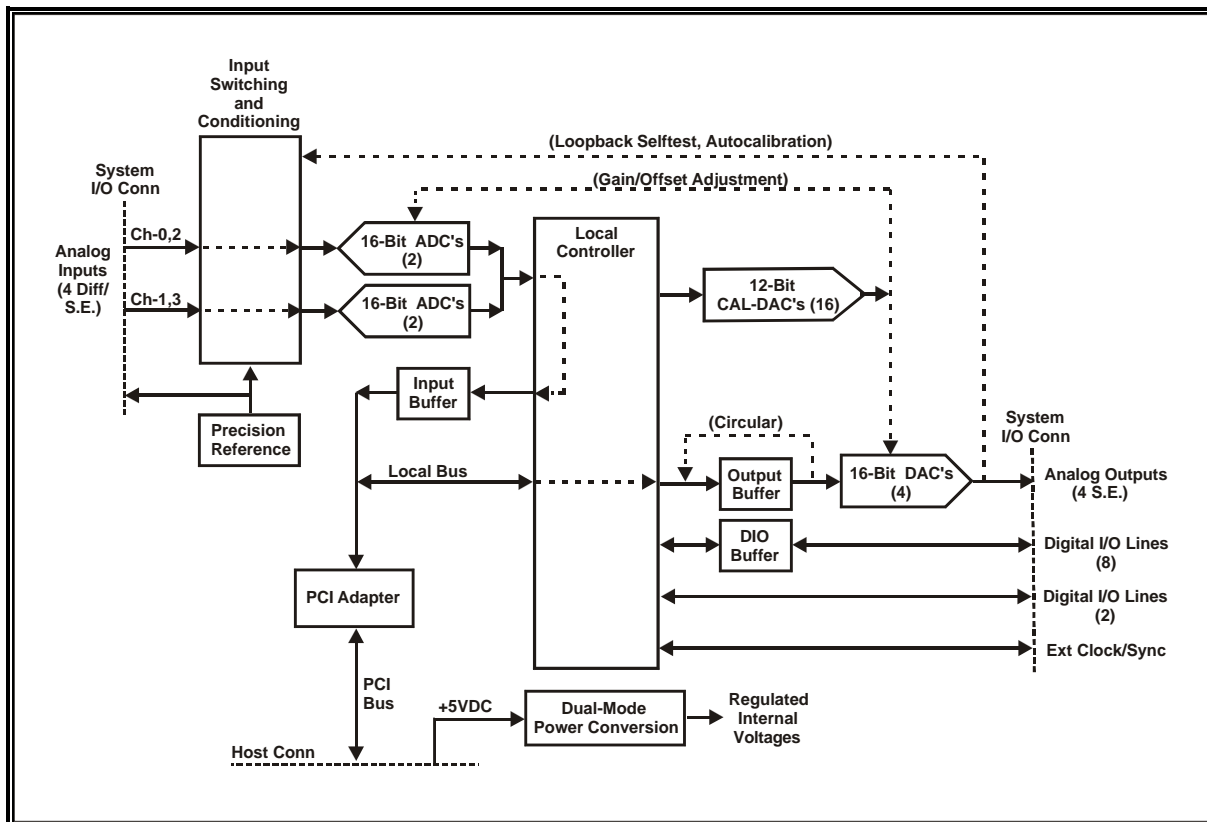


Figure 4.1-1. Functional Diagram

4.2 Control

A PCI interface adapter converts the control functions at the host interface into a local bus that is controlled in turn by a local controller. In addition to responding to host commands from the PCI interface adapter, the local controller performs all internal control operations for the module, including analog input/output clocking, data buffer access, digital I/O and autocalibration.

4.3 Electrical Power Conversion

Electrical power is obtained through the host interface as +5 VDC. To produce the various regulated power voltages that are required by the analog section of the module, the +5 VDC input is first converted by DC/DC switching converters into preregulated voltages that range from approximately ± 7 VDC to ± 18 VDC. These voltages then are postregulated to the final required levels by series regulators that ensure high-quality power rails.

4.4 Analog Inputs

Each of four analog input channels can be software-configured as either a differential or single-ended input, with a software-selected fullscale range of ± 2.5 V, ± 5 V or ± 10 V. The inputs can be sampled simultaneously at rates up to 1.0MSPS, or can be configured as sequenced pairs for effective sample rates as high as 2.0MSPS. Sequenced operation is implemented by clocking each ADC pair on alternate input clock cycles. Analog input channels are buffered through a dedicated analog input FIFO.

Analog input clocking can be derived from an internal rate generator or from an external hardware input, or can be controlled directly with a software clock. Both continuous and burst triggering modes are available.

During autocalibration, the response of each input channel is compared to precision internal voltages, and 12-bit calibration DAC's provide corrections for gain and offset errors. Autocalibration is executed on-demand by the host, and performs a 12-bit successive-approximation sequence of corrections to both the gain and offset errors of each analog channel. Final correction values are retained until the module is reset or power is removed. The calibration reference that is used during autocalibration is available for monitoring at a test pin in the system I/O connector.

4.5 Analog Outputs

Four analog output channels are driven from a dedicated FIFO buffer. The buffer can be clocked from a variety of sources, including an internal rate generator or an external hardware clock. The single-ended outputs can be operated with a software-selected fullscale range of ± 2.5 V, ± 5 V or ± 10 V, and can be clocked simultaneously at rates as high as 1.0MSPS. A remote ground-sensing input provides correction for potential differences between system grounds.

During autocalibration, each output is driven alternately to zero and fullscale. The corresponding output levels are compared with precision internal reference voltages to determine if the output is above or below the ideal values. Each output channel contains two 12-bit calibration DAC's for offset and gain corrections.

4.6 External Clock and Trigger

Both the clocking rates and trigger rates of analog input or output function bursts are software controlled through internal dividers that operate from the module's master clock. The outputs from each of these dividers can be replaced with an external digital input, which then controls the associated clock or trigger function.

Digital clock and trigger outputs permit multiple PMC modules to be clocked and triggered simultaneously by connecting the clock and trigger outputs from one module to the corresponding clock and trigger inputs of other modules in a daisy-chain sequence. One of the interconnected modules serves as a clock/trigger initiator, and the remaining modules perform as clock/trigger targets.

4.7 Digital Input/Output Port

The digital I/O port consists of eight bidirectional signals, one input-only signal, and one output-only signal. These digital signals are TTL compatible and use the host PCI bus ground as a digital return. All eight bidirectional signals are configured simultaneously as either inputs or outputs by the host, and are supported by a 1024-byte FIFO buffer. The buffer is clocked from an internal rate generator, and can be used to generate continuous, one-shot, or periodic bit patterns. The digital port also can be synchronized to analog input or output clocks.

APPENDIX A
SUPPLEMENTARY MATERIAL

