



PMC-3311

High-Speed 16-Channel 16-Bit PMC Analog Output Card With Aggregate Throughputs to 16 MSPS

FEATURES

- ◆ 16 SINGLE-ENDED ANALOG OUTPUTS
- ◆ 16-BIT D/A CONVERTER PER CHANNEL
- ◆ CLOCKING RATES TO 1.0 MSPS PER CHANNEL
- ◆ AGGREGATE THROUGHPUTS TO 16 MSPS
- ◆ SIMULTANEOUS OR INDEPENDENT CLOCKING
- ◆ PERIODIC OR CONTINUOUS SEQUENCING
- ◆ VOLTAGE RANGES $\pm 10V$, $\pm 5V$ OR $\pm 2.5V$
- ◆ DUAL 64-KSAMPLE OUTPUT FIFO BUFFERS
- ◆ TWO INDEPENDENT RATE GENERATORS
- ◆ DYNAMIC RATE CONTROL
- ◆ MASTERING DMA ENGINE
- ◆ MULTIBOARD SYNCHRONIZATION
- ◆ COMPREHENSIVE AUTO-CALIBRATION
- ◆ 8-BIT BIDIRECTIONAL DIGITAL I/O PORT
- ◆ COMPLETELY SOFTWARE-CONFIGURABLE
- ◆ SINGLE-WIDTH PMC FORM FACTOR

APPLICATIONS

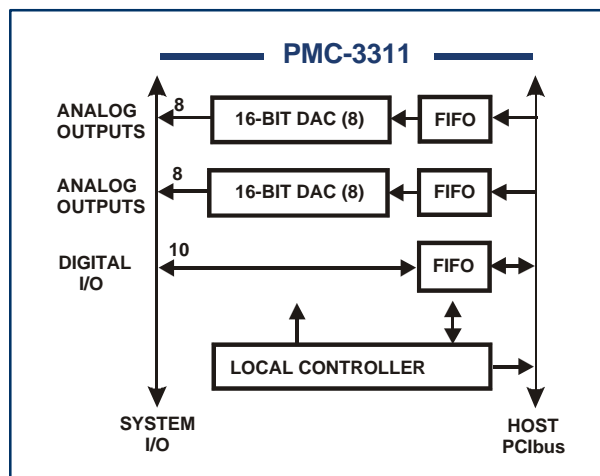
- FAST PRECISION ANALOG OUTPUTS
- ROBOTICS POSITIONING
- ARBITRARY WAVEFORM GENERATION
- FAST SERVO CONTROL LOOPS
- TEST SYSTEM STIMULI
- ACOUSTIC SIGNAL STREAMING
- WIDEBAND ANALOG OUTPUT
- HIGH RESOLUTION LITHOGRAPHY

With 16-Bit performance and aggregate throughputs up to 16 MSPS, the PMC-3311 provides superior analog output precision and bandwidth in a single-width PMC card. Sixteen individual 16-Bit D/A converters can be clocked at rates from zero to 1.0 MSPS (megasamples per second). The outputs can be clocked simultaneously or sequentially, or can be clocked as two independent channel groups.

Data can be streamed continuously to the outputs through two independent 64 K-sample FIFO's, or the FIFO's can be operated in circular mode for periodic function generation. Two independent FIFO's support the simultaneous generation of two independent function sets with separate clocks.

Output ranges can be supplied as $\pm 10V$, $\pm 5V$ or $\pm 2.5V$. Internal autocalibration and self-test ensure maximum accuracy under all conditions.

An 8-bit bidirectional I/O port can be controlled either directly or through a 256-Byte FIFO, and is supported by two auxiliary I/O lines.



Performance Specifications ¹

Analog Outputs

Outputs:	16 single-ended outputs. Optional 8 and 4-Channel versions available.
Organization:	Two 8-channel output groups, each operating from one of two independent FIFO buffers. The buffers can be clocked synchronously or independently from two internal rate generators, or from an external clock.
Resolution:	16 Bits; 0.0015 percent of FSR; DAC per channel
Voltage Ranges:	Factory-configured as ± 10 , ± 5 or ± 2.5 Volts
Loading:	Zero to ± 3 mA; Stable with up to 2000 pF shunt capacitance.
Output Impedance:	± 0.5 Ohms maximum
Clocking Rate:	Zero to 1.0 MSPS per channel; up to 16 MSPS aggregate clocking rate.
Settling Time:	4.0 μ S typical to 0.01 percent of half-scale step; 0-200 pF load capacitance
DC Accuracy, RTO	± 0.005 % Reading ± 0.003 % FSR ± 0.5 mV; E.g.: ± 1.0 mV with an output value of +4 Volts on the ± 5 V input range.
Crosstalk Rejection:	90dB, DC-100 Hz; 72 dB to 100kHz
Nonlinearity:	± 0.003 percent INL; ± 0.0015 percent DNL, maximum
Glitch Impulse:	10 nV-Sec on 2.5-Volt range, typical with MSB-transition
Noise:	1.0 mV-RMS typical; 10Hz to 1.0MHz.
Clocking Modes:	Simultaneous: All active outputs are clocked simultaneously. Sequential: Active channels are clocked sequentially.
Buffer Configuration:	Closed: The output buffer operates in circulating (looping) mode. Open: Data flows directly through the buffer to the outputs.
Burst Mode:	Triggered single-function (burst) mode.
Rate Generators:	Each of two independent 16-bit internal dividers provides clocking rates up to 1.0 MHz. Clocking from zero to 1.0 MHz can be supplied externally or through a local control register. Half of the output channels are assigned to each rate generator. Clocking rates can be controlled dynamically.
Output Data Buffers:	Two independent 64K-sample (optional 16K) FIFO's with adjustable threshold flag and DMA access. Half of the output channels are assigned to each buffer.

Compatibility

Compliance:	Conforms to the electrical requirements of PCI Local Bus Specification Revision 2.2, and to the IEEE 1386 standard for Common Mezzanine Cards (CMC).
Access Modes::	Read/Write D32; Single transaction as slave or DMA as master; Multifunction interrupt on INT-A.

Note 1: At +25°C, with specified environmental conditions.



Digital I/O Port

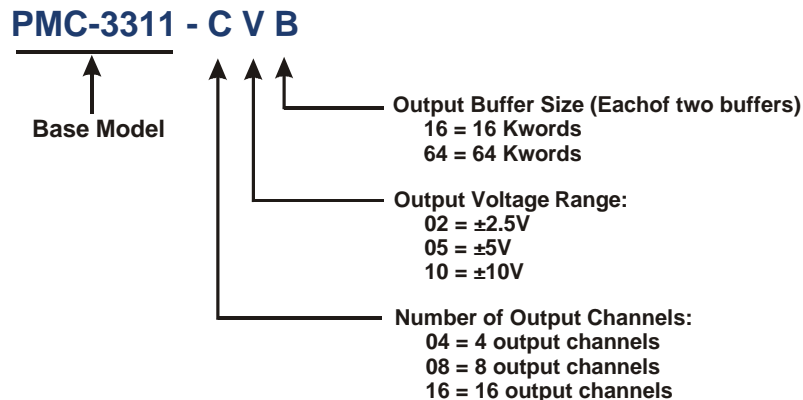
Configuration:	Bidirectional 8-Bit port with a FIFO buffer and two auxiliary I/O lines.
Logic Levels:	Standard TTL
Output Loading:	Zero to 20 ma, source and sink.
Access Modes:	Direct-Read/Write or Mastered DMA. Buffer orients automatically to support assigned port direction.
Buffer:	256-Byte FIFO buffer
Buffer Clocking Rate:	Zero to 18 MHz, controlled by internal rate generator or external clock.

Environmental Characteristics

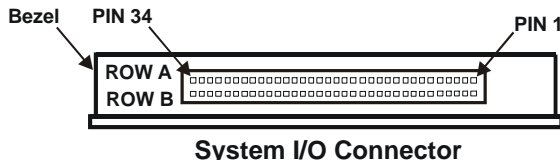
Dimensions:	HxWxD: 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 149.0 mm (5.87 in)	
Mass:	150 grams maximum	
Ambient Temperature:	Operating: 0 to +60 degrees Celsius;	Storage: -40 to +85 degrees
Humidity: (Noncondensing)	Operating: 0 to 85% RH;	Storage: 0 to 95% RH
Cooling:	150 LFPM air flow	
Altitude:	10,000 Feet (3000 Meters)	
Power Requirements:	+5 ±0.25 VDC at 1.3 Amps maximum	

Ordering Information

Specify base model number plus applicable option suffix as shown below:
For example; PMC-3311-160564 specifies 16 channels, ±5V outputs and 64K buffers:



System I/O Connections



Cable Mating Connector:

68-Pin 2-row 0.050" dual ribbon-cable socket connector:
Robinson Nugent # P50E-068-S-TG

PIN	FUNCTION	PIN	FUNCTION
1A	DIG RTN	1B	DIG RTN
2A	TRIG INPUT	2B	TRIG OUTPUT
3A	DIG RTN	3B	DIG RTN
4A	CLOCK INPUT	4B	CLOCK OUTPUT
5A	ANA RTN	5B	DIG RTN
6A	GROUND SENSE	6B	DIG IO 00
7A	OUTPUT RTN 00	7B	DIG RTN
8A	ANA OUT 00	8B	DIG IO 01
9A	OUTPUT RTN 01	9B	DIG RTN
10A	ANA OUT 01	10B	DIG IO 02
11A	OUTPUT RTN 02	11B	DIG RTN
12A	ANA OUT 02	12B	DIG IO 03
13A	OUTPUT RTN 03	13B	DIG RTN
14A	ANA OUT 03	14B	DIG IO 04
15A	OUTPUT RTN 04	15B	DIG RTN
16A	ANA OUT 04	16B	DIG IO 05
17A	OUTPUT RTN 05	17B	DIG RTN
18A	ANA OUT 05	18B	DIG IO 06
19A	OUTPUT RTN 06	19B	DIG RTN
20A	ANA OUT 06	20B	DIG IO 07
21A	OUTPUT RTN 07	21B	DIG RTN
22A	ANA OUT 07	22B	DIG RTN
23A	OUTPUT RTN 08	23B	DIG RTN
24A	ANA OUT 08	24B	DIG AUX INP
25A	OUTPUT RTN 09	25B	DIG RTN
26A	ANA OUT 09	26B	DIG AUX OUT
27A	OUTPUT RTN 10	27B	DIG RTN
28A	ANA OUT 10	28B	ANA RTN
29A	OUTPUT RTN 11	29B	OUTPUT RTN 13
30A	ANA OUT 11	30B	ANA OUT 13
31A	OUTPUT RTN 12	31B	OUTPUT RTN 14
32A	ANA OUT 12	32B	ANA OUT 14
33A	TEST OUT(-)	33B	OUTPUT RTN 15
34A	TEST OUT(+)	34B	ANA OUT 15

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