



PMC-2215

High-Speed 8-Channel 16-Bit PMC Analog Input/Output Card With 1.0MSPS Per Channel Input/Output Clocking and Software-Controlled Ranges

FEATURES

Analog Inputs:

- ◆ FOUR SINGLE-ENDED OR DIFFERENTIAL INPUTS
- ◆ 16-BIT A/D CONVERTER PER CHANNEL
- ◆ UP TO 1.0 MSPS PER CHANNEL (2.0 MSPS IN 2-CHANNEL SEQUENCED MODE)
- ◆ 4 MSPS AGGREGATE SAMPLE RATE
- ◆ SIMULTANEOUS OR SEQUENCED SAMPLING
- ◆ CONTINUOUS AND BURST TRIGGERING

Analog Outputs:

- ◆ FOUR SINGLE-ENDED ANALOG OUTPUTS
- ◆ 16-BIT D/A CONVERTER PER CHANNEL
- ◆ CLOCKING RATES TO 1.0 MSPS/CHANNEL
- ◆ SIMULTANEOUS OR SEQUENTIAL CLOCKING
- ◆ DYNAMIC RATE CONTROL

Common Features:

- ◆ VOLTAGE RANGES $\pm 10V$, $\pm 5V$, $\pm 2.5V$
- ◆ 64-KSAMPLE INPUT/OUTPUT BUFFERS
- ◆ INTERNAL RATE GENERATORS
- ◆ MASTERING DMA ENGINE
- ◆ COMPREHENSIVE AUTOCALIBRATION
- ◆ 8-BIT BIDIRECTIONAL DIGITAL I/O PORT

APPLICATIONS

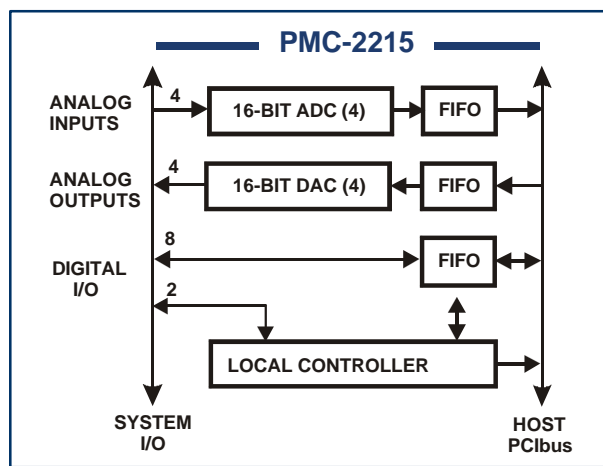
- FAST PRECISION ANALOG INPUT/ OUTPUT
- ROBOTICS POSITIONING AND MONITORING
- ARBITRARY WAVEFORM GENERATION
- RADAR SYSTEMS
- ACOUSTICS AND AUDIO
- WIDEBAND SERVO CONTROL
- EVENT CAPTURE

The PMC-2215 provides exceptional 16-bit analog input/output performance on a standard single-width PMC card. Quad 16-Bit A/D converters sample four input channels simultaneously at up to 1.0MSPS, and support both continuous and burst triggering modes. The inputs can be clocked as four simultaneous channels, or as two sequenced pairs to effectively double the maximum sampling rate to 2MSPS per channel.

Four 16-Bit D/A converters provide four output channels with simultaneous or sequential clocking at rates up to 1.0 MSPS/channel, for an aggregate rate of 4.0 MSPS. The output clocking rate can be controlled dynamically from within an output function.

Inputs and outputs can be software-configured with $\pm 10V$, $\pm 5V$ or $\pm 2.5V$ ranges, and are accessed through two independent 64-Ksample deep-FIFO buffers. Internal autocalibration and selftest ensure maximum accuracy at all times.

An 8-Bit bidirectional digital I/O port and two auxiliary digital I/O lines support pattern generation with a 1024-Word byte-wide FIFO buffer.



PRELIMINARY



Performance Specifications ¹

Analog Inputs

Inputs:	Four input pairs, configurable as four single-ended or differential channels; ADC per channel. Optional two-Channel version available.
Resolution:	16 Bits; 0.0015 percent of FSR; ADC per channel
Voltage Ranges:	Software configurable as ± 10 , ± 5 or ± 2.5 Volts; same as output range.
Sample Rate:	0-1.0MSPS; 0-2.0MSPS for two channels with sequenced sampling.
Bandwidth:	Small signal: DC to 2.5 MHz, minimum. Slew Rate: 12 V/us typical.
DC Accuracy, RTI	± 0.006 % Reading ± 0.004 % FSR ± 0.5 mV; E.g.: ± 1.14 mV when reading +4 Volts on the ± 5 V input range.
Crosstalk Rejection:	88dB, DC-10kHz; 85 dB to 100kHz, 80dB to 400kHz, typical
Nonlinearity:	± 0.004 percent INL; ± 0.0015 percent DNL, maximum
Dynamics:	SFDR*: 90 dB, THD: 90 dB; typical with 180 kHz, 0.3 FSR-RMS.
Input Noise:	SNR: 87dB 10Hz - 100kHz, typical. 80dB to 500kHz. 4dB lower in sequenced sampling mode.
Input Impedance:	1.0 Megohm pull-down resistors on all input lines.
Common Mode :	CMRR: 75 dB typical, DC-60 Hz, differential input mode. ± 10 V CMV.
Overvoltage:	Withstands ± 30 Volts with power applied; ± 15 Volts with power removed
Sampling Modes:	Simultaneous: All four inputs are sampled simultaneously. Sequenced: Inputs are clocked as sequenced pairs, with each pair sampled every other input clock. Effectively doubles the maximum per-channel input sample rate.
Trigger Modes:	Continuous: Samples are acquired continuously. Burst: Samples are acquired in triggered bursts.
Clocking Modes:	Internal rate generator or external source. Analog inputs and outputs can be clocked independently or synchronously.
Selftest Support	Input channels monitor output channels or internal references.
Input Data Buffer:	64K-sample (optional 16K) FIFO with DMA access and adjustable threshold flag.

* Spurious-free dynamic range.

Analog Outputs

Outputs:	Four single-ended outputs; Two-Channel version available.
Resolution:	16 Bits; 0.0015 percent of FSR; DAC per channel
Voltage Ranges:	Software configurable as ± 10 , ± 5 or ± 2.5 Volts; same as input range.
DC Accuracy, RTO:	± 0.007 % Reading ± 0.005 % FSR ± 0.5 mV (unloaded); E.g.: ± 1.28 mV with an output of +4-volts on the ± 5 V input range. Add ± 500 uV per mA of load current.
Loading:	Zero to ± 5 mA; Stable with up to 2000 pF shunt capacitance.

Note 1: At +25°C. After autocalibration, with specified environmental



Analog Outputs (Continued)

Clocking Rate:	Zero to 1.0 MSPS per channel
Settling Time:	3.0 uS max to 0.01 percent of half-scale step; 0-200 pF load capacitance
Crosstalk Rejection:	92dB, DC-100 Hz; 73 dB to 100 kHz
Nonlinearity:	±0.003 percent INL; ±0.0015 percent DNL, maximum
Transition Impulse:	10 nV-Sec on 2.5-Volt range, with MSB-transition
Output Impedance:	0.5 Ohms maximum
Noise:	1.0 mV-RMS typical; 10 Hz to 1.0 MHz.
Clocking Modes:	Simultaneous: All active outputs are clocked simultaneously. Sequential: Active channels are clocked sequentially. Clocking source can be an internal rate generator or an external clock.
Buffer Configuration:	Closed: The output buffer operates in circulating (looping) mode. Open: Data flows directly through the buffer to the outputs.
Burst Mode:	Triggered single-function (burst) mode. Internal and external triggering.
Output Data Buffer:	64K-Sample or 16K FIFO with DMA access and adjustable threshold flag.

Digital I/O Port

Configuration:	Bidirectional 8-Bit port with a FIFO buffer and two auxiliary I/O lines
Logic Levels:	Standard TTL
Output Loading:	Zero to 20 ma, source and sink
Access Modes:	Direct-Read/Write or mastered DMA. Buffer orients automatically to support assigned port direction
Buffer:	1024-Byte FIFO buffer
Buffer Clocking Rate:	Zero to 18 MHz, controlled by internal rate generator or external clock

Environmental Characteristics

Dimensions:	HxWxD: 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 149.0 mm (5.87 in)
Mass:	150 grams maximum
Ambient Temperature:	Operating: 0 to +60 degrees Celsius; Storage: -40 to +85 degrees
Humidity: (Noncondensing)	Operating: 0 to 85% RH; Storage: 0 to 95% RH
Cooling:	150 LFPM air flow
Altitude:	10,000 Feet (3000 Meters)
Power Requirements:	+5 ±0.25 VDC at 1.2 Amps maximum, 0.9 Amps typical.

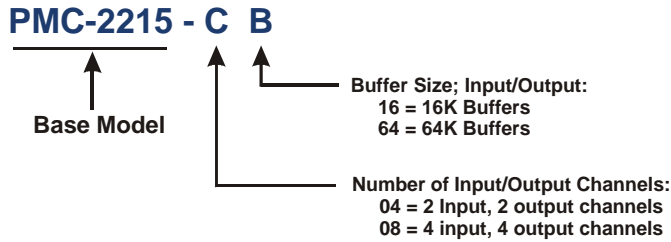
Compatibility

Compliance:	Conforms to the electrical requirements of PCI Local Bus Specification Revision 2.2, and to the IEEE 1386 standard for Common Mezzanine Cards (CMC).
Access Modes:::	Read/Write D32; Single transaction as slave or DMA as master; Multifunction interrupt on INT-A.

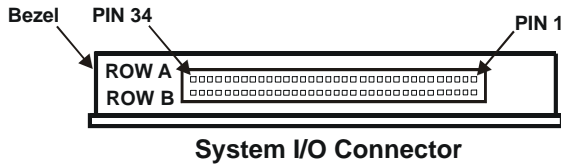


Ordering Information

Specify base model number plus applicable option suffix as shown below:
 For example; PMC-2215-0864 specifies eight I/O channels and 64K buffers:



System I/O Connections



Cable Mating Connector:

68-Pin 2-row 0.050" dual ribbon-cable socket connector:
 Robinson Nugent # P50E-068-S-TG

PIN	FUNCTION	PIN	FUNCTION
1A	DIG RTN	1B	DIG RTN
2A	ADC TRIG INPUT	2B	ADC TRIG OUTPUT
3A	DIG RTN	3B	DIG RTN
4A	ADC CLOCK INPUT	4B	ADC CLOCK OUTPUT
5A	DIG RTN	5B	DIG RTN
6A	DAC TRIG INPUT	6B	DAC TRIG OUTPUT
7A	DIG RTN	7B	DIG RTN
8A	DAC CLOCK INPUT	8B	DAC CLOCK OUTPUT
9A	OUTPUT RTN	9B	DIG RTN
10A	GROUND SENSE	10B	DIG IO 00
11A	OUTPUT RTN	11B	DIG RTN
12A	ANA OUT 00	12B	DIG IO 01
13A	OUTPUT RTN	13B	DIG RTN
14A	ANA OUT 01	14B	DIG IO 02
15A	OUTPUT RTN	15B	DIG RTN
16A	ANA OUT 02 *	16B	DIG IO 03
17A	OUTPUT RTN	17B	DIG RTN
18A	ANA OUT 03 *	18B	DIG IO 04
19A	INP RTN	19B	DIG RTN
20A	INP RTN	20B	DIG IO 05
21A	ANA INP LO 00	21B	DIG RTN
22A	ANA INP HI 00	22B	DIG IO 06
23A	INP RTN	23B	DIG RTN
24A	INP RTN	24B	DIG IO 07
25A	ANA INP LO 01	25B	DIG RTN
26A	ANA INP HI 01	26B	DIG AUX 01 (Input)
27A	INP RTN	27B	DIG RTN
28A	INP RTN	28B	DIG AUX 02 (Output)
29A	ANA INP LO 02 *	29B	DIG RTN
30A	ANA INP HI 02 *	30B	DIG RTN
31A	INP RTN	31B	INP RTN
32A	INP RTN	32B	INP RTN
33A	ANA INP LO 03 *	33B	TEST OUT(-)
34A	ANA INP HI 03 *	34B	TEST OUT(+)

* 8-Channel cards only

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